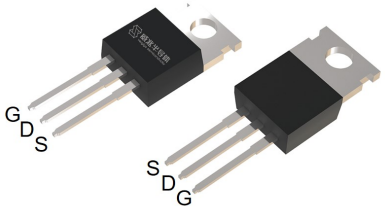
V_{DS}	30	V
$R_{DS(on),TYP}$@ V_{GS}=10 V	2.1	mΩ
$R_{DS(on),TYP}$@ V_{GS}=4.5 V	2.8	mΩ
I_D	180	A

Features

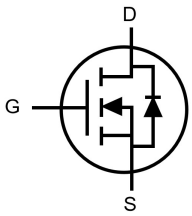
- N-Channel，5V Logic Level Control
- Enhancement mode
- Very low on-resistance $R_{DS(on)}$ @ V_{GS}=4.5 V
- 100% Avalanche Tested
- Pb-free lead plating; RoHS compliant

TO-220AB



Pb-Free RoHS HF Halogen-Free

Part ID	Package Type	Marking	Packing
VS3604AT	TO-220AB	3604AT	50pcs/Tube



Maximum ratings, at T_A=25 °C, unless otherwise specified

Symbol	Parameter		Rating	Unit
$V_{(BR)DSS}$	Drain-Source breakdown voltage		30	V
VGS	Gate-Source voltage		±20	V
I_S	Diode continuous forward current	T_C=25°C	180	A
I_D	Continuous drain current @V_{GS}=10V	T_C=25°C	180	A
		T_C=100°C	127	A
I_{DM}	Pulse drain current tested ①	T_C=25°C	720	A
I_{DSM}	Continuous drain current @VGS=10V	T_A=25°C	24	A
		T_A=70°C	19	A
EAS	Avalanche energy, single pulsed ②		169	mJ
P_D	Maximum power dissipation	T_C=25°C	115	W
P_{DSM}	Maximum power dissipation ③	T_A=25°C	2	W
T_{STG}, T_J	Storage and Junction Temperature Range		-55 to 175	°C

Thermal Characteristics

Symbol	Parameter	Typical	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	1.3	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	62.5	°C/W

Copyright© Vergiga Semiconductor Co., Ltd

Electrical Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Static Electrical Characteristics @ T_j = 25°C (unless otherwise stated)						
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D=250μA	30	--	--	V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=30V,V_{GS}=0V	--	--	1	μA
	Zero Gate Voltage Drain Current(T_j=125℃)	V_{DS}=30V,V_{GS}=0V	--	--	100	μA
I_{GSS}	Gate-Body Leakage Current	V_{GS}=±20V,V_{DS}=0V	--	--	±100	nA
$V_{GS(TH)}$	Gate Threshold Voltage	V_{DS}=V_{GS},I_D=250μA	1.3	1.8	2.4	V
$R_{DS(ON)}$	Drain-Source On-State Resistance ④	V_{GS}=10V, I_D=40A	--	2.1	3	mΩ
$R_{DS(ON)}$	Drain-Source On-State Resistance ④	V_{GS}=4.5V, I_D=20A	--	2.8	4	mΩ
Dynamic Electrical Characteristics @ T_j= 25°C (unless otherwise stated)						
C_{iss}	Input Capacitance	V_{DS}=15V,V_{GS}=0V, f=1MHz	3500	4565	5500	pF
C_{oss}	Output Capacitance		570	785	1000	pF
C_{rss}	Reverse Transfer Capacitance		500	710	900	pF
R_g	Gate Resistance	f=1MHz	--	3.6	--	Ω
Q_g	Total Gate Charge	V_{DS}=15V,I_D=40A, V_{GS}=10V	--	73	--	nC
Q_{gs}	Gate-Source Charge		--	12	--	nC
Q_{gd}	Gate-Drain Charge		--	18	--	nC
Switching Characteristics						
$t_{d(on)}$	Turn-on Delay Time	V_{DD}=15V, I_D=40A, R_G=3Ω, V_{GS}=10V	--	12	--	ns
t_r	Turn-on Rise Time		--	8.5	--	ns
$t_{d(off)}$	Turn-Off Delay Time		--	77.5	--	ns
t_f	Turn-Off Fall Time		--	19.5	--	ns
Source- Drain Diode Characteristics@ T_j = 25°C (unless otherwise stated)						
V_{SD}	Forward on voltage	I_{SD}=40A,V_{GS}=0V	--	0.8	1.2	V
t_{rr}	Reverse Recovery Time	T_j=25℃,I_{sd}=40A, V_{GS}=0V di/dt=500A/μs	--	31	--	ns
Q_{rr}	Reverse Recovery Charge		--	15.5	--	nC

NOTE:

① Repetitive rating; pulse width limited by max junction temperature.

② Limited by T_{Jmax}, starting T_J = 25°C, L = 0.5mH,R_G = 25Ω, I_{AS} = 26A, V_{GS} =10V. Part not recommended for use above this value

③ The power dissipation P_{DSM} is based on $R_{\theta JA}$ and the maximum allowed junction temperature of 150°C.

④ Pulse width ≤ 300μs; duty cycle≤ 2%.

Copyright© Vergiga Semiconductor Co., Ltd

Typical Characteristics

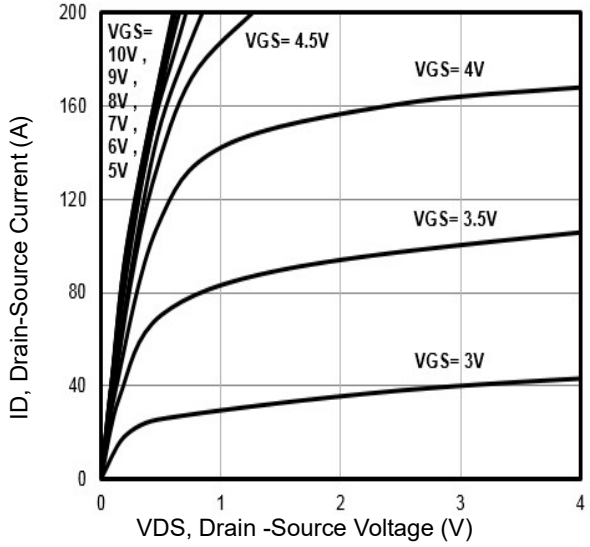


Fig1. Typical Output Characteristics

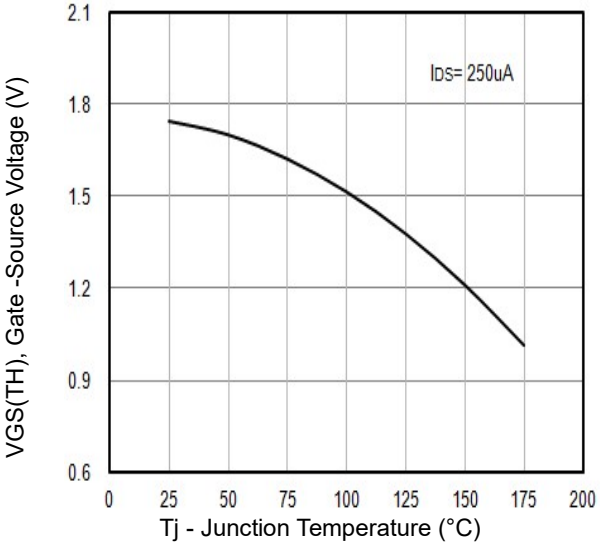


Fig2. $V_{GS(TH)}$ Gate -Source Voltage Vs. Tj

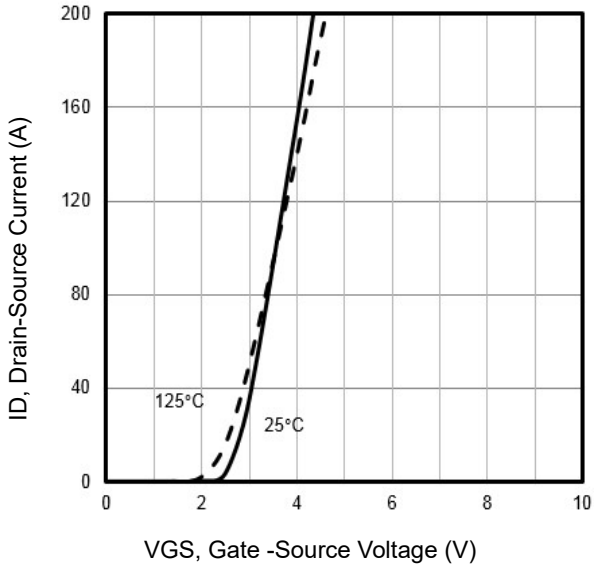


Fig3. Typical Transfer Characteristics

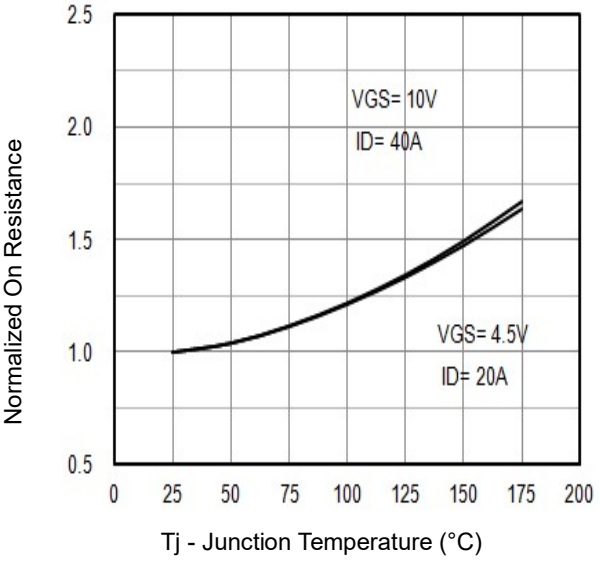


Fig4. Normalized On-Resistance Vs. Temperature

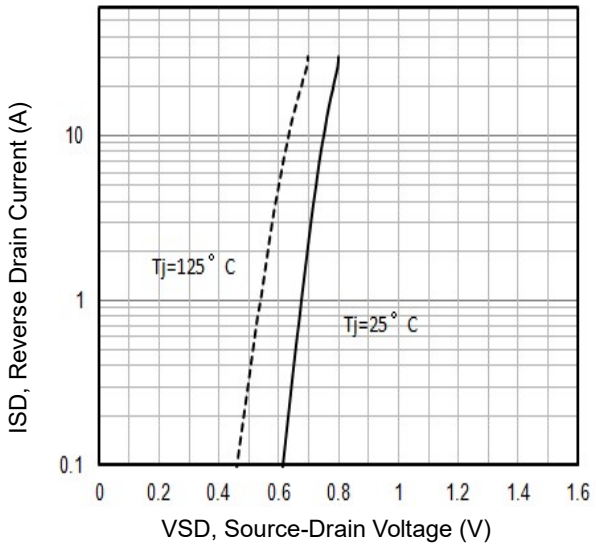


Fig5. Typical Source-Drain Diode Forward Voltage

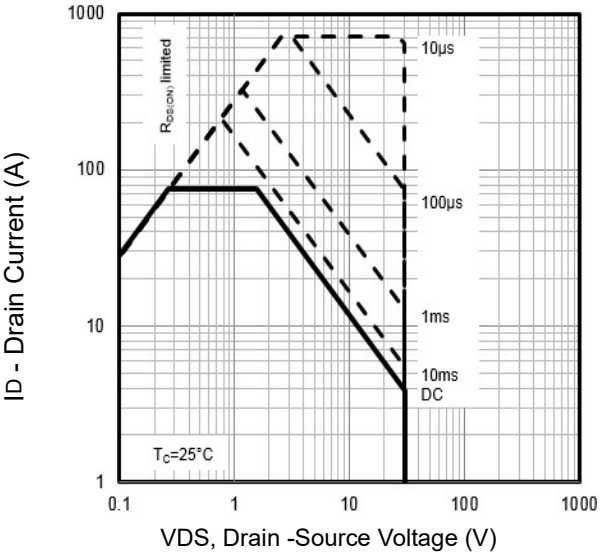


Fig6. Maximum Safe Operating Area

Copyright© Vergiga Semiconductor Co., Ltd

Typical Characteristics

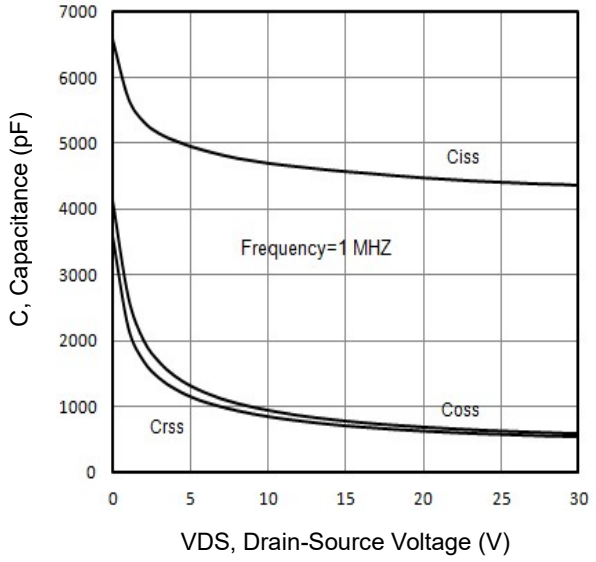


Fig7. Typical Capacitance Vs. Drain-Source Voltage

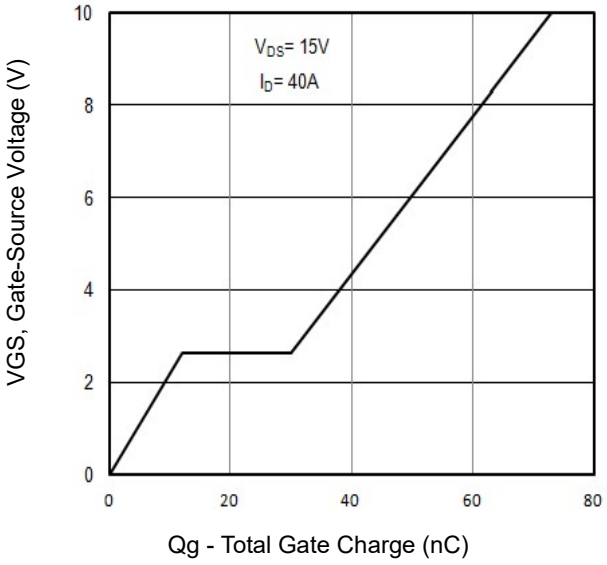


Fig8. Typical Gate Charge Vs. Gate-Source Voltage

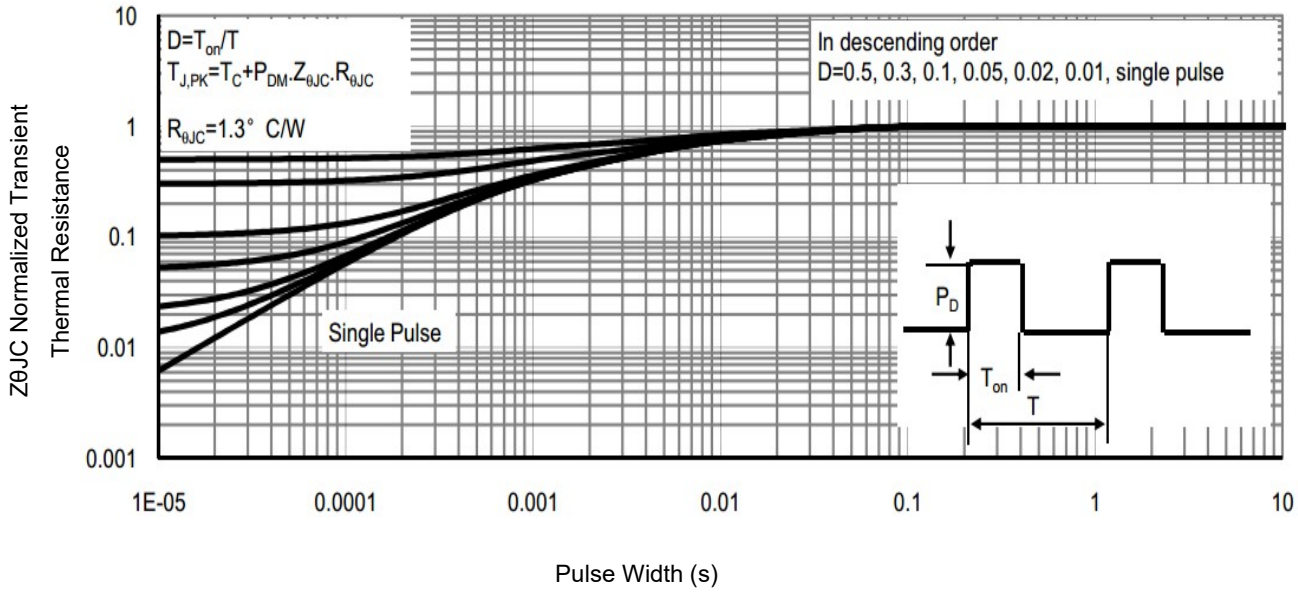


Fig9. Normalized Maximum Transient Thermal Impedance

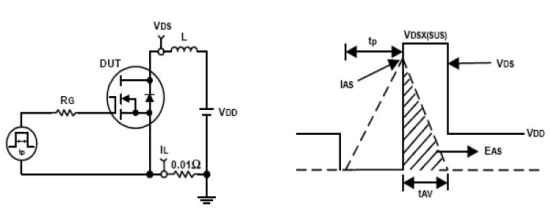


Fig10. Unclamped Inductive Test Circuit and waveforms

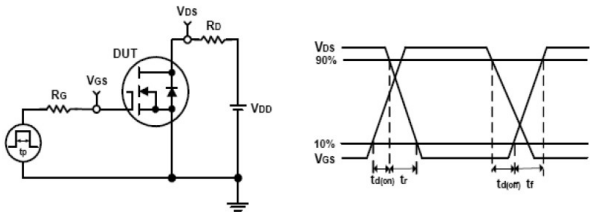
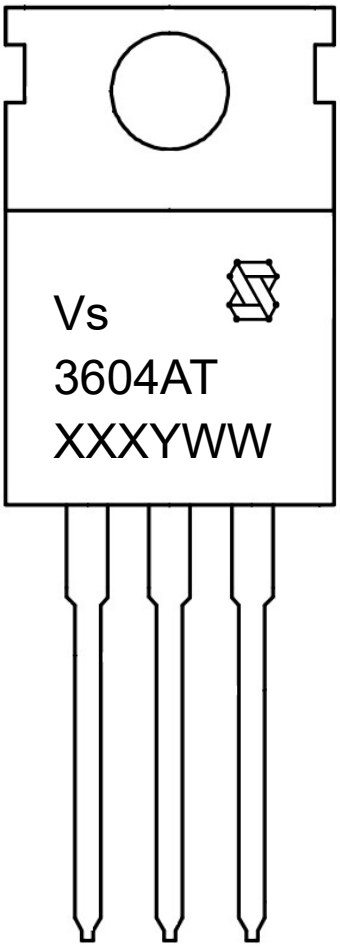


Fig11. Switching Time Test Circuit and waveforms

Copyright© Vergiga Semiconductor Co., Ltd

Marking Information

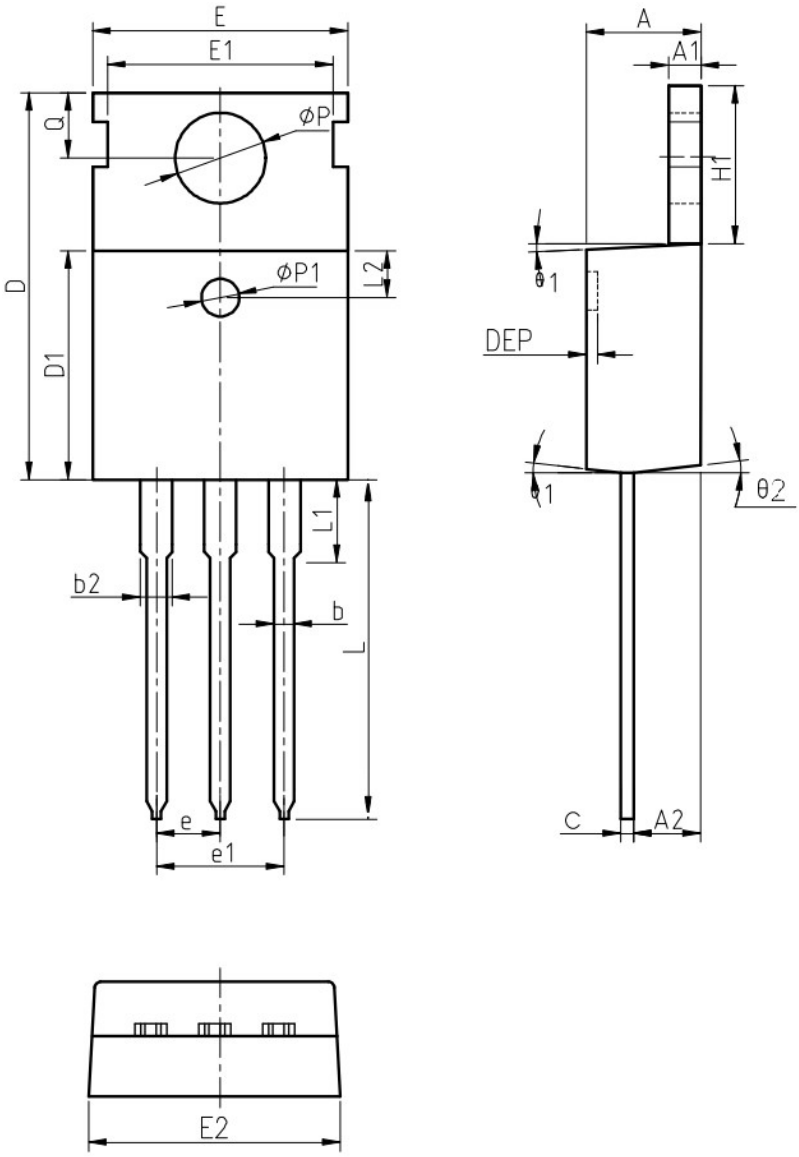


1st line: Vergiga Code（Vs），Vergiga Logo
2nd line: Part Number（3604AT）
3rd line: Date code （XXXYWW）
XXX: Wafer Lot Number Code , code changed with Lot Number
Y: Year Code ， refer to table below
WW: Week Code (01 to 53)

Code	C	D	E	F	G	H	J	K	L	M	N	P	Q	R	S	T
Year	2015	2016	2017	2018	2019	2020	2021	2022	2023	2024	2025	2026	2027	2028	2029	2030

Copyright© Vergiga Semiconductor Co., Ltd

TO-220AB Package Outline Data



Symbol	Dimensions (unit: mm)		
	Min	Typ	Max
A	4.30	4.52	4.70
A1	1.15	1.30	1.40
A2	2.20	2.40	2.60
b	0.70	0.80	1.00
b2	1.17	1.32	1.50
c	0.45	0.50	0.61
D	15.30	15.65	15.90
D1	9.00	9.20	9.40
DEP	0.05	0.10	0.25
E	9.66	9.90	10.28
E1	-	8.70	-
E2	9.80	10.00	10.20
ΦP1	1.40	1.50	1.60
e	2.54 BSC		
e1	5.08 BSC		
H1	6.40	6.50	6.80
L	12.70	-	14.27
L1	-	-	3.95
L2	2.40	2.50	2.60
ΦP	3.53	3.60	3.70
Q	2.70	2.80	2.90
θ1	5 °	7 °	9 °
θ2	1 °	3 °	5 °

Notes:

1. Refer to JEDEC TO-220 variation AB
2. Dimension "D" and "E" do NOT include mold flash. Mold flash shall not exceed 0.127mm per side.

Customer Service

Sales and Service:

sales@vgsemi.com

Vergiga Semiconductor CO., LTD

TEL: (86-755) -26902410

FAX: (86-755) -26907027

WEB: **www.vgsemi.com**

Copyright© Vergiga Semiconductor Co., Ltd