16-bit constant current LED driver with operating supply of 3.3V to 5V

T B 6 2 7 2 6 A F N A

Data Sheet Version No.	Date	Note	Inspect
001	2002-4-26	Target spec by AFNA	
002	2002-5-15	The setup of the tentative Spec of Iout	
003	2002-5-21	Evaluation set of Iout Spec.	
004	2002-5-28	The reflection of the test Spec.	
005	2002-6-1	Some of proofreading	
006	2002-6-22	Some of proofreading	
007	2002-10-1	A format is changed.	
008	2002-10-11	IOUT Spec. reexamination	
009	2002-11-6	Final Spec.	

We agree this specification.

Company Date

Signature

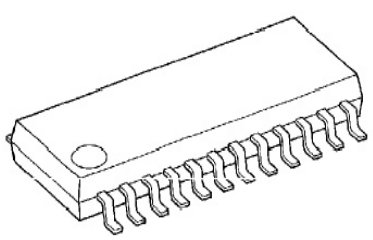
TOSHIBA Bi-CMOS INTEGRATED CIRCUIT SILICON MONOLITHIC

T B 6 2 7 2 6 A F N A

16-bit constant current LED driver with operation supply of 3.3V to 5V

The TB62726AFNA is comprised of constant-current drivers designed for LEDs and LED displays. The output current value can be set using an external resistor. As a result, all outputs will have virtually the same current levels. This driver incorporates a 16-bit constant-current output, a 16-bit shift register, a 16-bit latch and a gate circuit. These drivers have been designed using the Bi-CMOS process.

TB62726AFNA



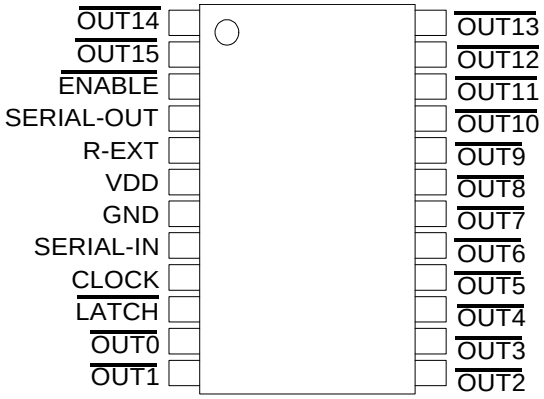
P-SSOP24-150-0.635

Feature

*Output current capability and the number of output:
90 mA x 16 outputs
*Constant current range : 2 to 90 mA
*Application output voltage :
0.7V (output current 2 to 80mA)
0.4V (output current 2 to 40mA)
*For anode common LED
*Input signal voltage level :
3.3V-5.0V CMOS level (schmitt trigger input)
*Power supply voltage range VDD=3.0 to 5.5V
*Muximum output terminal voltage 17V
*Serial and parallel data transfer rate 20 MHz (min., Cascade Connection)
*Operation temperature range topr = -40 to 85 degrees
*Package : P-SSOP24-150-0.635
*Current accuracy (not used dot-current correction.)

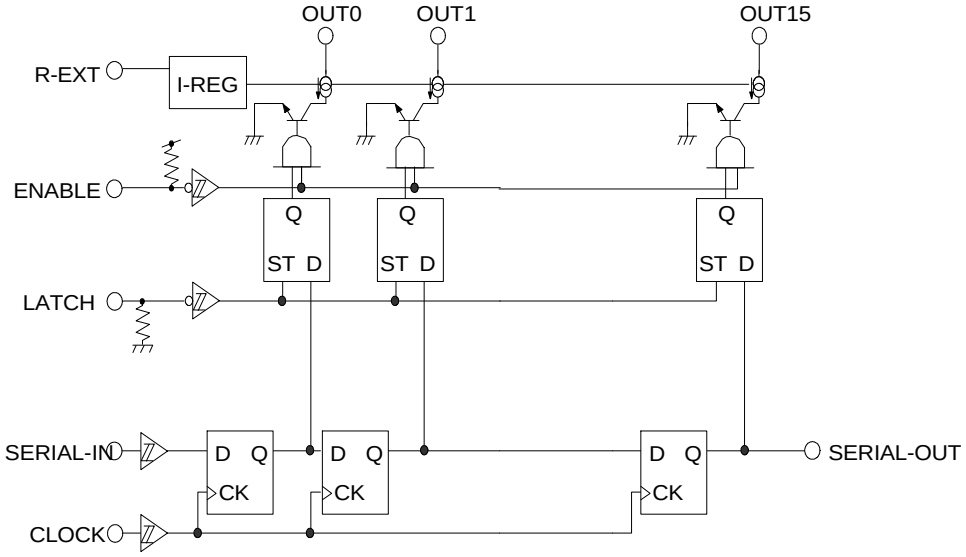
Output voltage	Current accuracy		Output current
	between bits	between ICs	
>= 0.4V	+/- 4 %	+/- 12 %	2 to 40 mA
>= 0.7V			2 to 90 mA

Package and pin layout (Top view)



Warnings : Short-circuiting an output terminal to GND or to the power supply terminal may broken the device.
Please take care when wiring the output terminals, the power supply terminal and the GND terminals.

Block Diagram

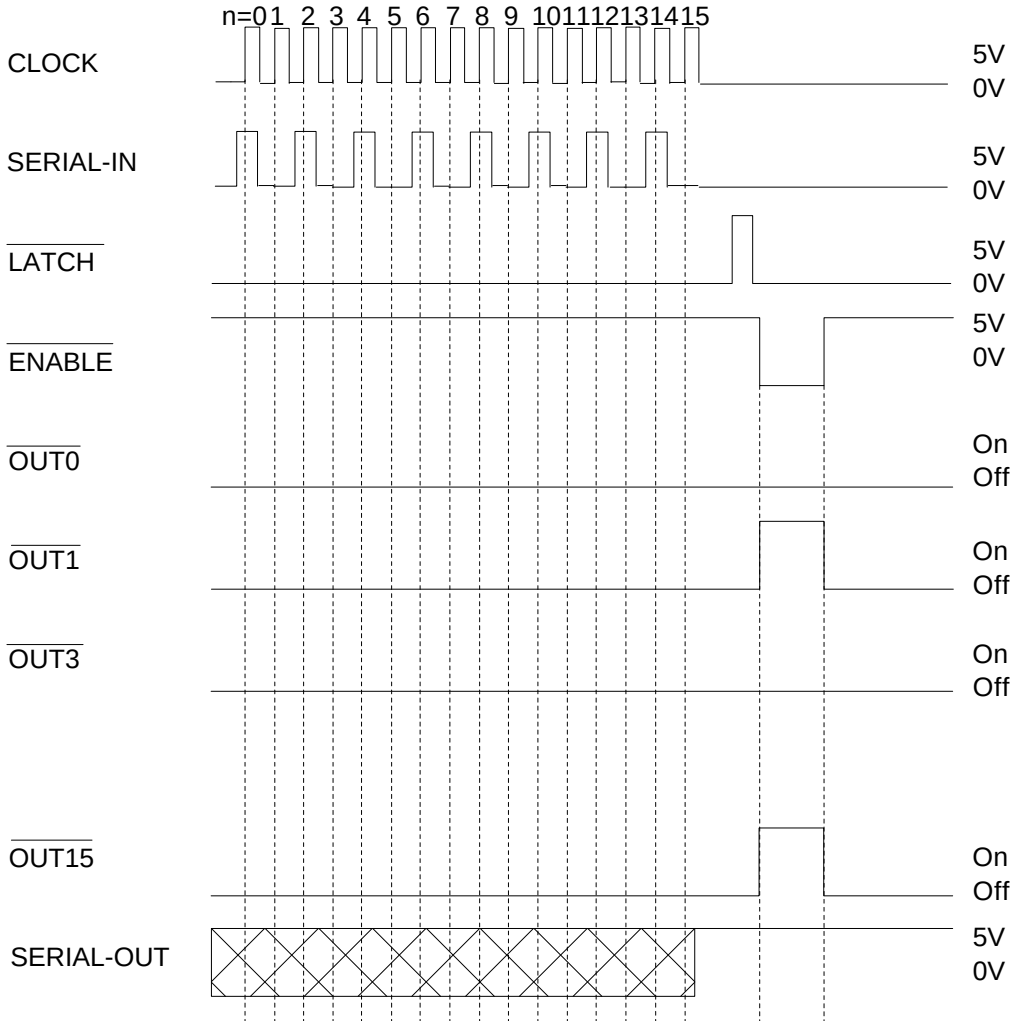


Truth Table

CLOCK	LATCH	ENABLE	SERIAL-IN	OUT0 --- OUT7 --- OUT15	SERIAL-OUT
Positive edge	H	L	Dn	Dn --- Dn-7 --- Dn-15	Dn-15
Positive edge	L	L	Dn+1	No Change	Dn-14
Positive edge	H	L	Dn+2	Dn+2 --- Dn-5 --- Dn-13	Dn-13
Negative edge	X	L	Dn+3	Dn+2 --- Dn-5 --- Dn-13	Dn-13
Negative edge	X	H	Dn+3	Off	Dn-13

Note 1: OUT0~OUT15=ON when Dn=H ; OUT0~OUT15=OFF when Dn=L
In order to ensure that the level of the power supply voltage is correct, an external resistor have to connected between R-EXT and GND.

Timing diagram



Warning :

Latch circuit is leveled-latch circuit. Be careful because it is not triggered-latch circuit.

Note 2 :

The latches circuit holds data by pulling the LATCH terminal Low. And, when LATCH terminal is a High-level, latch circuit doesn't hold data, and it passes from theInput to the output. When ENABLE terminal is Low-level, output terminal OUT0~OUT15 respond to the data, and on & off does.

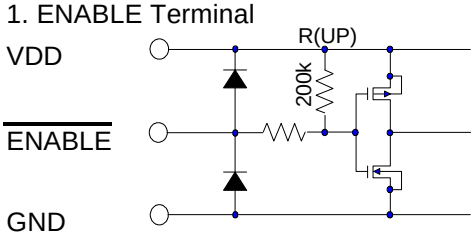
And, when ENABLE terminal is a High-level, it offs with the output terminal regardless of the data.

Terminal description

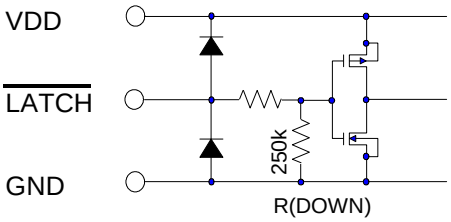
Pin No.	Pin Name	Function
7	GND	GND terminal for control logic
8	SERIAL-IN	Input terminal for serial data for data shift register
9	CLOCK	Input terminal for clock for data shift on rising edge
10	$\overline{\text{LATCH}}$	Input terminal for data strobe When the LATCH=High-level, data is no latched. When ithe LATCH=Low-level, data is latched.
1 to 2, 11 to 24	$\overline{\text{OUT 0 to 7}}$	Constant-current output terminals
3	$\overline{\text{ENABLE}}$	Input terminal for output enable. All outputs (OUT0 ~ OUT15) are turned off, when the ENABLE=High-level. And are turned on, when the ENABLE=Low-level.
4	SERIAL-OUT	Output terminal for serial data input on SERIAL-IN terminal
5	R-EXT	Input terminal used to connect an external resistor. This regulated the output current.
6	VDD	3.3V - 5V supply voltage terminal.

Equivalent circuit of inputs and output

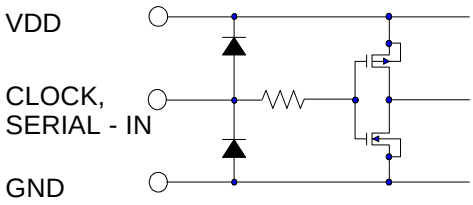
1. $\overline{\text{ENABLE}}$ Terminal



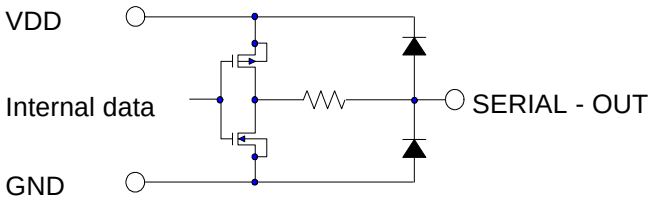
2. $\overline{\text{LATCH}}$ Terminal



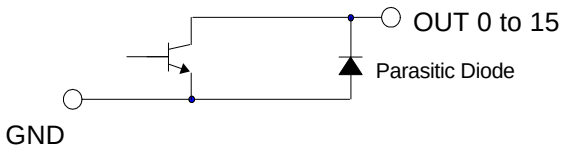
3. CLOCK,SERIAL-IN Terminal



4. SERIAL-OUT Terminal



5. OUT0 to 15 Terminal



Absolute maximum ratings

Characteristics	Symbol	Rating	Unit
Supply Voltage	V_{DD}	+6	V
Input Voltage	V_{IN}	-0.2 to VDD+0.2	
Output Current	I_{OUT}	+90	mA/ch
Output Voltage	V_{OUT}	-0.2 to 17	V
Power Dissipation	P_d1	0.89	W
Thermal Resistance	$R_{th(j-a)}$	140 (Free Air)	degree/W
Operating Temperature	T_{opr}	-40 to 85	degree
Storage Temperature	T_{stg}	-55 to 150	

Note 3 : Subtract 7.10mW/degree every time an ambient temperature exceeds 25 times once.

Recommended operating condition (VDD=4.5~5.5V, Topr = -40~85 degree, unless otherwise noted.)

Characteristics	Symbol	Condition	Min	Typ	Max	Unit
Supply Voltage	V_{DD}	-	3	-	5.5	V
Output Voltage	V_{OUT}(On)	-	-	0.7	4	V
Output Current	I_{OUT}	Each DC 1 Circuit	2	-	80	mA/ch
	I_{OH}	SERIAL-OUT	-	-	-1	mA
	I_{OL}		-	-	1	
Input Voltage	V_{IH}	-	0.7xVDD	-	VDD+0.15	V
	V_{IL}		-0.15	-	0.3xVDD	
Clock Frequency	f_{CLK}	Cascade Connected	-	-	20	MHz
LATCH Pulse Width	$t_{w\ LATCH}$		50	-	-	ns
CLOCK Pulse Width	$t_{w\ CLOCK}$		25	-	-	
ENABLE Pulse Width When the pulse of the Low level is inputted to the ENABLE terminal held in the H level.	$t_{w\ ENABLE}$	Upper I_{OUT}=20mA	2000	-	-	
		Lower I_{OUT}=20 mA	3000	-	-	
Setup Time for CLOCK Terminal	$t_{SETUP}1$	-	10	-	-	
			10	-	-	
Hold Time for CLOCK Terminal	t_{HOLD}		50	-	-	
Setup Time for /LATCH Terminal	$t_{SETUP}2$					

Electrical characteristics (VDD=3V to 5.5V, Topr=25degree unless otherwise noted.)

Characteristics	Symbol	Condition		Min	Typ	Max	Unit
Supply voltage	V_{DD}	Normal operation		3.0	-	5.5	V
Output current	$I_{OUT}1$	V_{OUT}=0.4V,V_{DD}=3.3V	R_{EXT}= 490 ohm	31.96	36.20	40.54	mA
	$I_{OUT}2$	V_{OUT}=0.4V,V_{DD}=5V		31.59	35.90	40.20	
	$I_{OUT}3$	V_{OUT}=0.7V,V_{DD}=3.3V	R_{EXT}= 250 ohm	63.63	72.30	80.97	
	$I_{OUT}4$	V_{OUT}=0.7V,V_{DD}=5V		62.75	71.30	79.95	
Output current error between bits	$d_{IOUT}1$	V_{OUT}=0.4V, R_{EXT}=490 ohm	All output ON	-	+/-1	+/-4	%
	$d_{IOUT}2$	V_{OUT}=0.4V, R_{EXT}=250 ohm					
Output leakage Current Input voltage	I_{OZ}	V_{OUT}=15V		-	-	1	uA
Input voltage	V_{IN}	-		0.7VDD	-	VDD	V
		-		GND	-	0.3VDD	
SOUT terminal Voltage	V_{OL}	I_{OL}=+1 mA, Vdd=3.3V		-	-	0.3	V
		I_{OL}=+1 mA, Vdd=5V		-	-	0.3	
	V_{OH}	I_{OH}=-1 mA, Vdd=3.3V		3	-	-	
		I_{OH}=+1 mA,Vdd=5V		4.7	-	-	
Output current supply voltage regulation	%/V_{DD}	When V_{DD} is changed 3V to 5.5V		-	-1	-5	%/V
Pull up resistor	$R_{(UP)}$	ENABLE terminal		115	230	460	Ohm
Pull down resistor	$R_{(DOWN)}$	LATCH terminal					
Supply current	$I_{DD(OFF)}1$	R_{EXT}=Open, V_{OUT}=15V		-	0.1	0.5	
	$I_{DD(OFF)}2$	R_{EXT}=490ohm	All output OFF, V_{OUT}=15V	1	3.5	5	
	$I_{DD(OFF)}3$	R_{EXT}=250ohm		4	6	9	
	$I_{DD(ON)}1$	R_{EXT}=490ohm	All output ON, V_{OUT}=0.7V	-	9	15	
		Ta= -40degree, Same as the avobe.		-	-	20	
	$I_{DD(ON)}2$	R_{EXT}=250ohm	All output ON, V_{OUT}=0.7V	-	18	25	
		T_a= -40 degree, Same as the avobe.		-	-	40	

Switching characterictics (Topr=25degree, unless otherwise noted)

Characteristics	Symbol	Condition	Min	Typ	Max	Unit
Propagation delay	$t_{pLH}1$	CLK-OUTn, LATCH="H", ENABLE="L"	-	150	300	ns
	$t_{pLH}2$	LATCH-OUTn, ENABLE="L"	-	140	300	
	$t_{pLH}3$	ENABLE-OUTn, LATCH="H"	-	140	300	
	t_{pLH}	CLK-SERIALOUT	3	6	-	
	$t_{pHL}1$	CLK-OUTn, LATCH="H", ENABLE="L"	-	170	340	
	$t_{pHL}2$	LATCH-OUTn, ENABLE="L"	-	170	340	
	$t_{pHL}3$	ENABLE-OUTn, LATCH="H"	-	170	340	
	t_{pLH}	CLK-SERIAL-OUT	4	7	-	
Output rise time	t_{or}	Voltage waveform 10%~90%	40	85	150	
Output fall time	t_{of}	Voltage waveform 90%~10%	40	70	150	
Maximum CLK rise time	t_r	When not on PCB	-	-	5	us
Maximum CLK fall time	t_f		-	-	5	

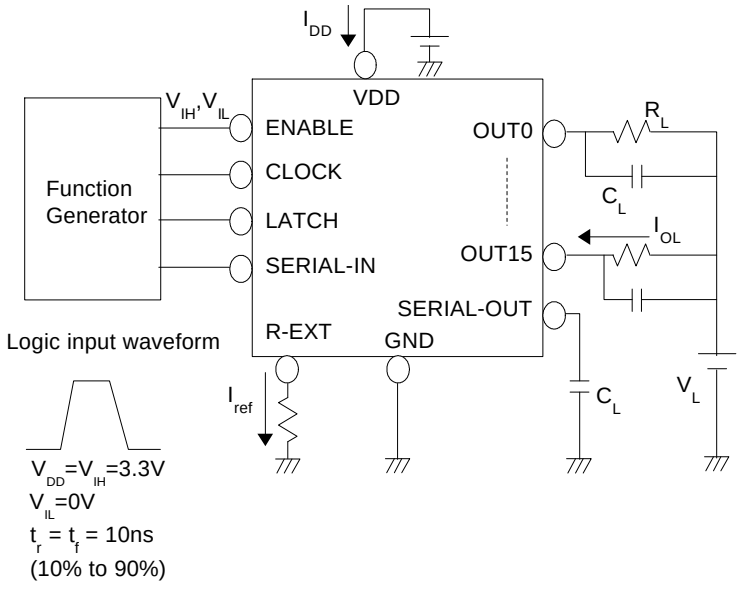
Condition : (Refer to test circuit)

Topr=25 degree, V_{DD}=V_{IH}=3.3V and 5V, V_{OUT}=0.7V, V_{IL}=0V,R_{EXT}=490ohms, V_L=3.0V, R_L=60ohms,C_L=10.5pF

Note 4 :

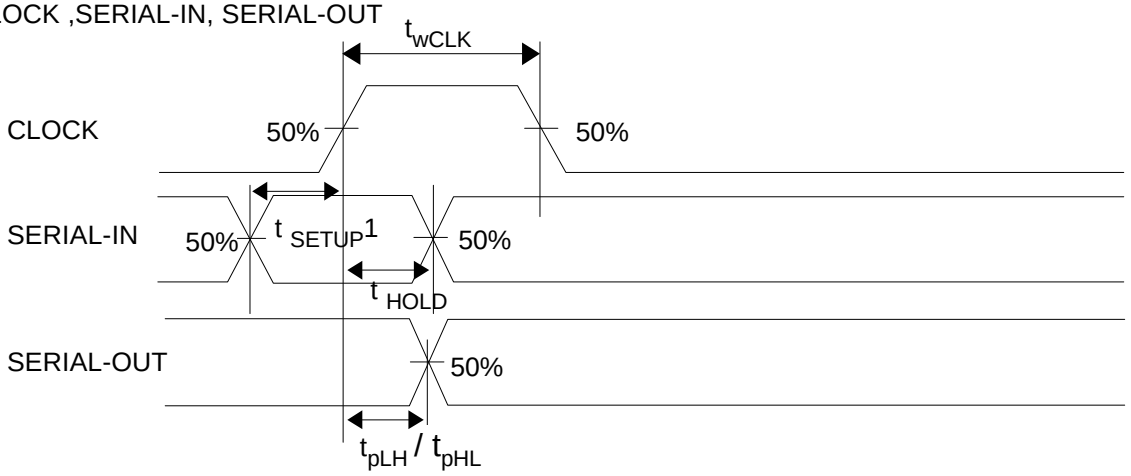
If the device is connected in a cascade and tr/tf for the waveform is large, it may not be possible to achieve the timing required for data transfer. Please consider the timings carefully.

Test circuit

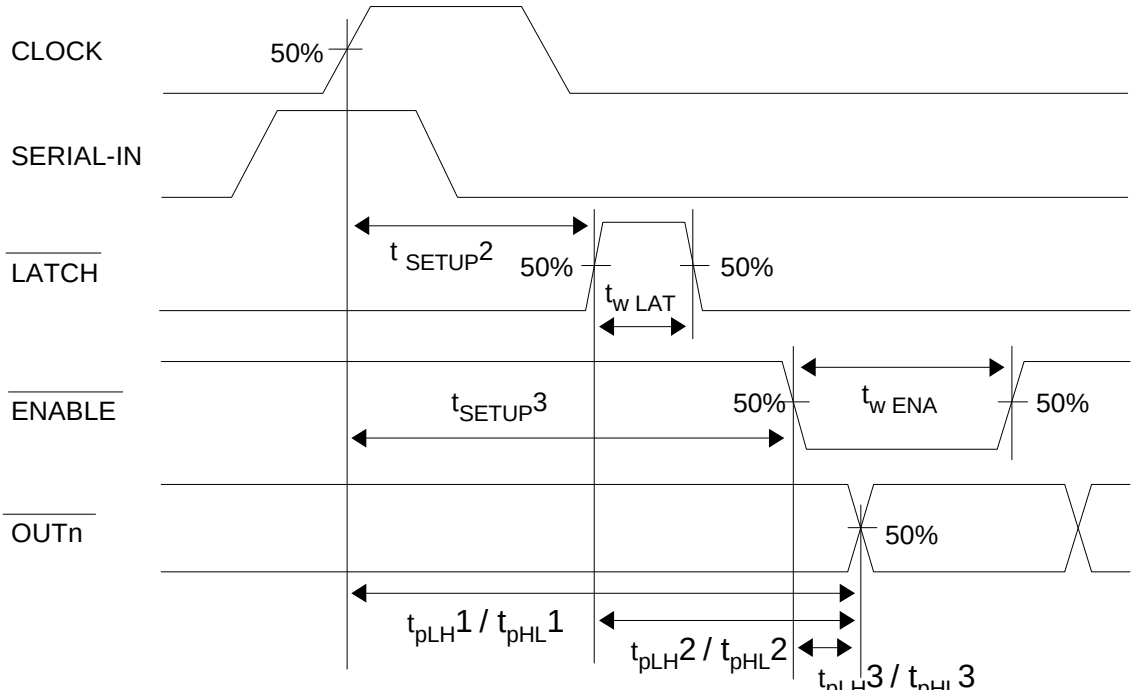


Timing Waveform

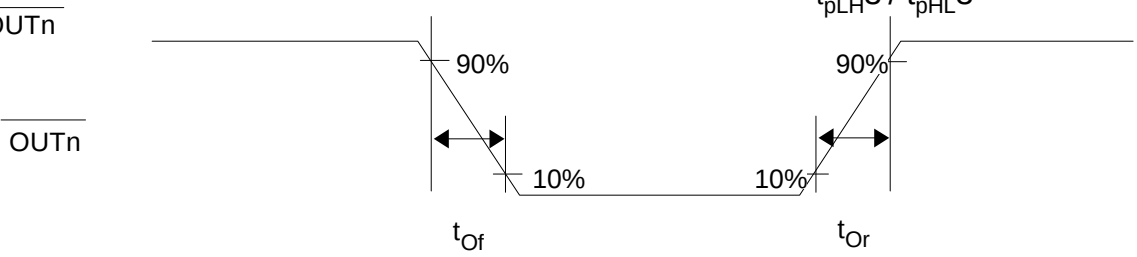
1. CLOCK ,SERIAL-IN, SERIAL-OUT



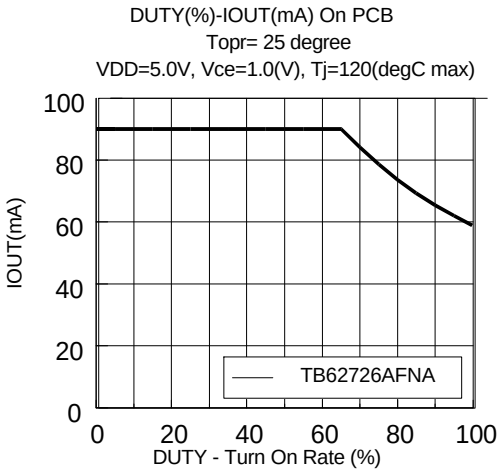
2. CLOCK, SERIAL-IN , $\overline{\text{LATCH}}$, $\overline{\text{ENABLE}}$, $\overline{\text{OUTn}}$

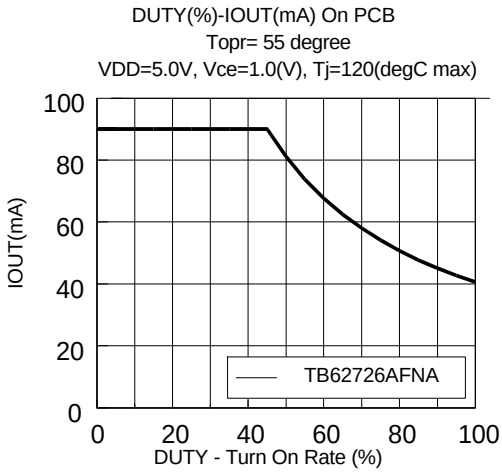


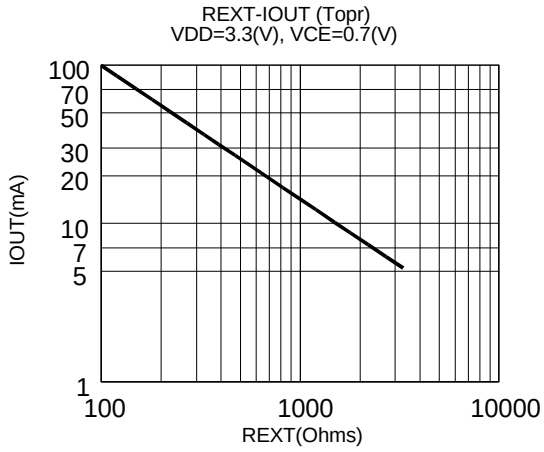
3. $\overline{\text{OUTn}}$

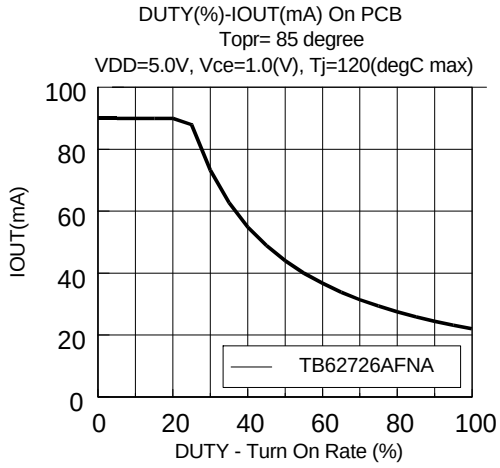


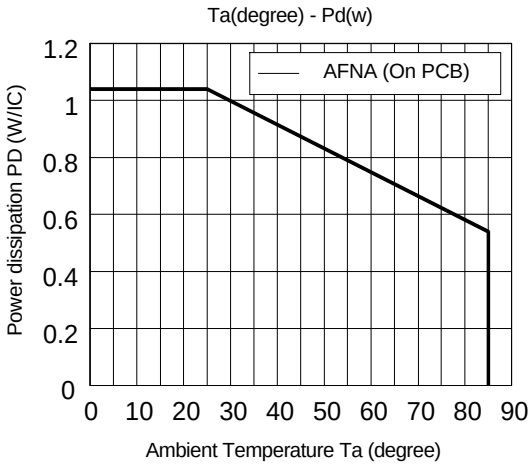
Output current vs duty (LEDs turn on rate)







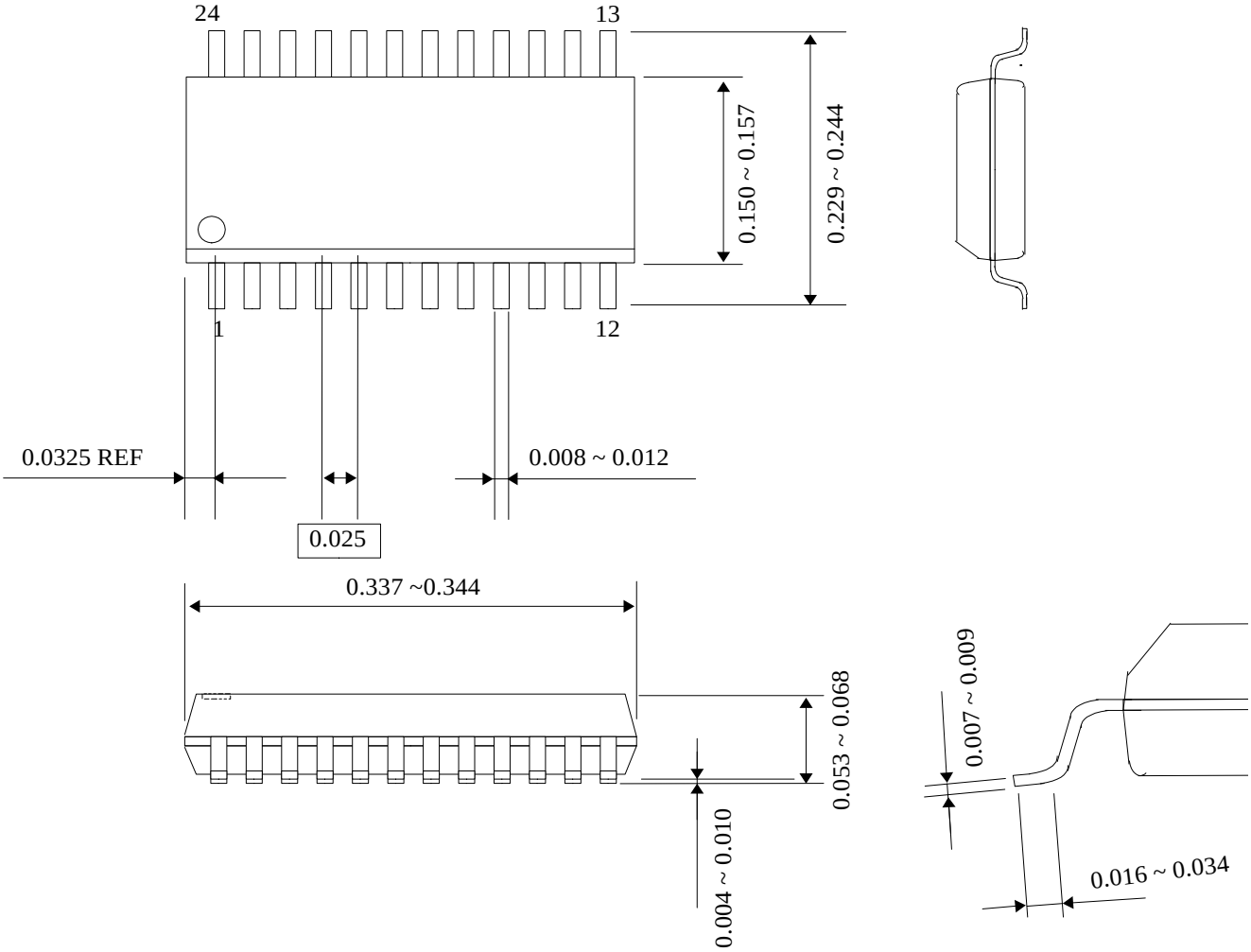




Package dimmension P-SSOP24-150-0.635

UNIT : Inch

TENTATIVE



The information contained herein is subject to change without notice.

The information contained herein is presented only as a guide for the applications of our products. No responsibility is assumed by TOSHIBA for any infringements of patens or other rights of the third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of TOSHIBA or others.

TOSHIBA is continually working to improve the quality and the reliability of its products. Nevertheless, semiconductor devices in general can malfunction or fail due to their inherent electrical sensitivity and vulnerability to physical stress. It is the responsibility of the buyer, when utilizing TOSHIBA products, to observe standards of safety, and to avoid situations in which a malfunction or failure of a TOSHIBA product could cause loss of human life, bodily injury or damage to property.
In developing your designs, please ensure that TOSHIBA products are used within spacified operating ranges as set forth in the most recent products spacifications. Also, please keep in mind the precautions and conditions set forth in the TOSHIBA Semiconductor Reliability Handbook.

The products described in the document may include products subject to foreign exchange and foreign trade control laws.

(C) 2000-2002 TOSHIBA CORPORATION
ALL RIGHT Reserved