RTR6285™/RTR6280™ RF Transceiver IC
Device Specification (Advance Information)

80-VD861-1 Rev. E

October 20, 2007

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Revision history

Revision	Date	Description
A	December 2006	Initial release
B	April 2007	Added information about RTR6280 throughout document Updated Figure 4-1 (RTR6285 IC functional block diagram) Added Figure 1-2 (RTR6280 IC functional block diagram) Added Figure 2-2 (RTR IC pin assignments (top view)) Updated Table 3-2 (Recommended operating conditions) Added Table 3-3 (Current consumption) Updated Table 3-5 (GSM 850/900 receive signal path specifications) Updated Table 3-6 (GSM 1800/1900 receive signal path specifications) Updated Figure 4-1 (68 mQFN package outline drawing) Updated Figure 4-2 (RTR6285 device marking) Added Figure 4-3 (RTR6280 device marking) Updated Table 4-1 (Device marking line descriptions) Updated Figure 6-1 (68 mQFN land and stencil pattern drawing)
C	September 2007	Put document into updated device specification template. Updates throughout Chapter 3, Electrical Specifications – TBD information was supplied for Table 3-1, Table 3-2, Table 3-3, Table 3-5, Table 3-6, Table 3-7, Table 3-8, Table 3-9, Table 3-12, Table 3-13, Table 3-17, and Table 3-18.
D	September 2007	Updated Pin 10 label in Figure 2-2 Updated Pin 10 in Table 2-2 Updated Residual sideband level value in Table 3-5 Updated Typ values in Table 4-3
E	October 2007	Updated HW ID for RTR6285 product version 13, sample 3 in Table 4-1 Updated HW ID for RTR6280 product version 01, sample 2 in Table 4-2

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1 Overview

1.1 Documentation overview

This document is part of a set of documents that describes the QUALCOMM RTR6285/RTR6280 RFIC and how best to use it. The RTR6285/RTR6280 device supports quadband UMTS (bands 1 through 6 and bands 8 through 9), quadband GSM/EDGE, GPS (RTR6285 only), and UMTS diversity(RTR6285 only) handset operation with direct conversions between RF and baseband using zero-IF (ZIF) radio architectures.

Technical RTR6285/RTR6280 IC information is distributed over four documents (Table 1-1). Each is a self-contained document, but thorough understanding of the IC and its applications requires studying all four. The device description given in the next section is a good place to start. All released RTR6285/RTR6280 documents are posted on the QCT external website (https://downloads.cdmatech.com) and are available for download.

Table 1-1 RTR6285/RTR6280 documents

Doc. no.	Title and description
80-VD861-1 (this document)	*RTR6285/RTR6280 RF Transceiver IC Device Specification* The primary objective of this document is to convey all RTR6285/RTR6280 electrical and mechanical specifications. Additional information includes pin assignment definitions, PCB mounting specifications, packing methods and materials, and part reliability. This document can be used by company purchasing departments to facilitate procurement.
80-VD861-3	*RTR6285/RTR6280 RF Transceiver IC User Guide* This document provides detailed descriptions of all RTR6285/RTR6280 functions and interfaces, defining how to control the IC and explaining the resulting operating modes.
80-VD861-6	*radioOne® Platform-F/G (RFCMOS)Chipset Design Guidelines* This document tries to anticipate and answer questions hardware engineers might have when incorporating the radioOne 6285/6280 F/G series RF chipset into their product designs. Example applications are presented and specific design topics such as layout guidelines, power distribution recommendations, external component recommendations, troubleshooting techniques (and more) are addressed.
80-VD861-4	*RTR6285/RTR6280 RF Transceiver IC Revision Guide* This document provides a history of RTR6285/RTR6280 IC revisions and changes to its device specification. It explains how to identify the various IC revisions, discusses known issues (or bugs) for each revision and how to work around them, and lists performance specification changes between each revision of the *RTR6285/RTR6280 RF Transceiver IC Device Specification*.

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This RTR6285/RTR6280 device specification is organized as follows:

Chapter 1	Provides an overview of RTR6285/RTR6280 documentation, gives a high-level functional description of the RTR6285/RTR6280 IC, lists the device features, and lists terms and acronyms used throughout this document
Chapter 2	Defines the IC pin assignments
Chapter 3	Defines the IC electrical performance specifications, including absolute maximum ratings and recommended operating conditions
Chapter 4	Defines the IC mechanical specifications, including dimensions, thermal characteristics, moisture sensitivity, and markings
Chapter 5	Presents procedures and specifications for mounting the RTR6285/RTR6280 IC on printed circuit boards (PCBs)
Chapter 6	Discusses packing methods and materials for RTR6285/RTR6280 shipments
Chapter 7	Presents RTR6285/RTR6280 IC reliability data, including definition of the qualification samples and a summary of qualification test results

1.2 Device description

The RTR6285/RTR6280 device is a highly integrated radio frequency complementary metal oxide semiconductor (RF CMOS) transceiver IC.

The functional block diagram for the RTR6285 IC is shown in Figure 1-1 and the functional block diagram for the RTR6280 IC is shown in Figure 1-2.

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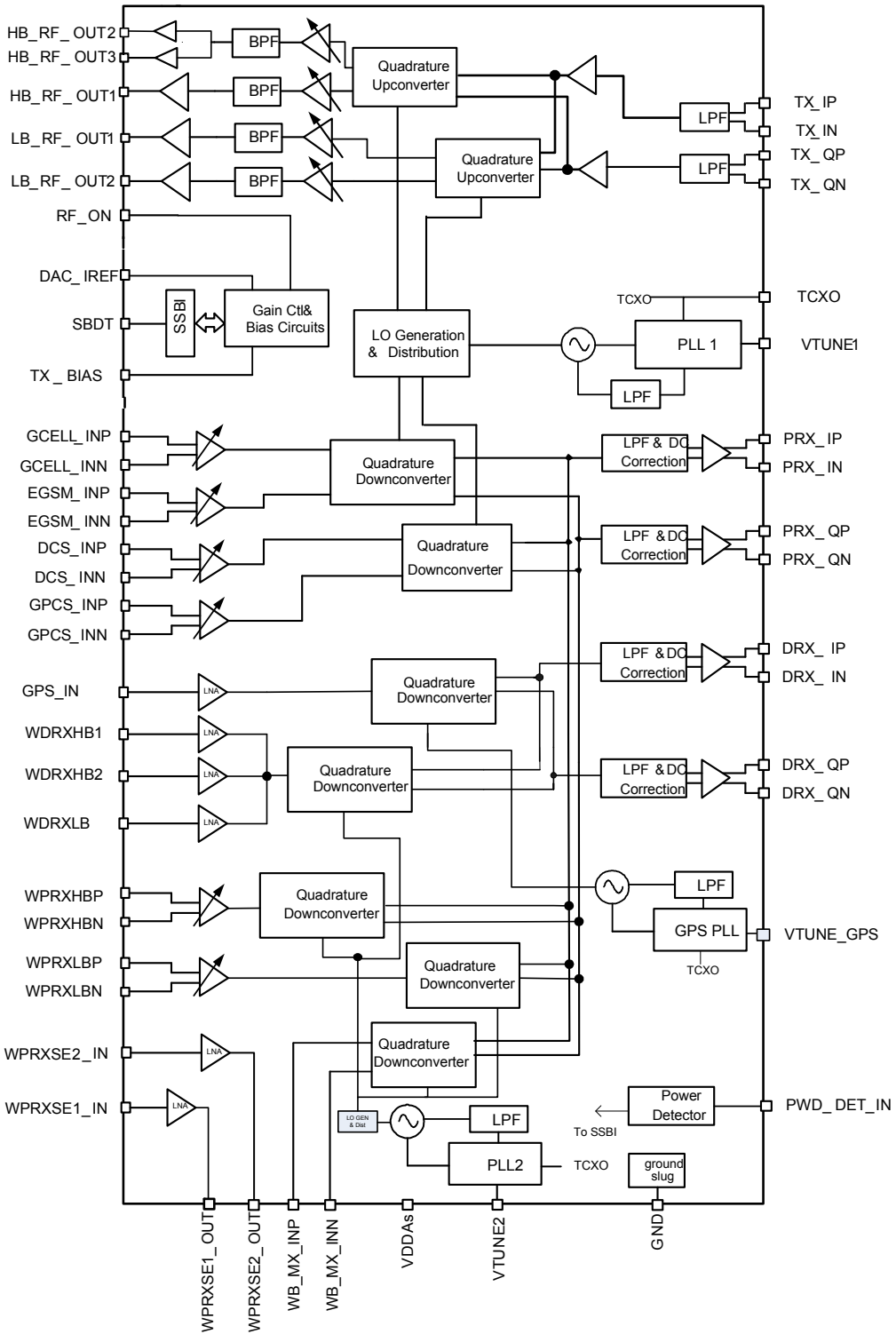


Figure 1-1 RTR6285 IC functional block diagram

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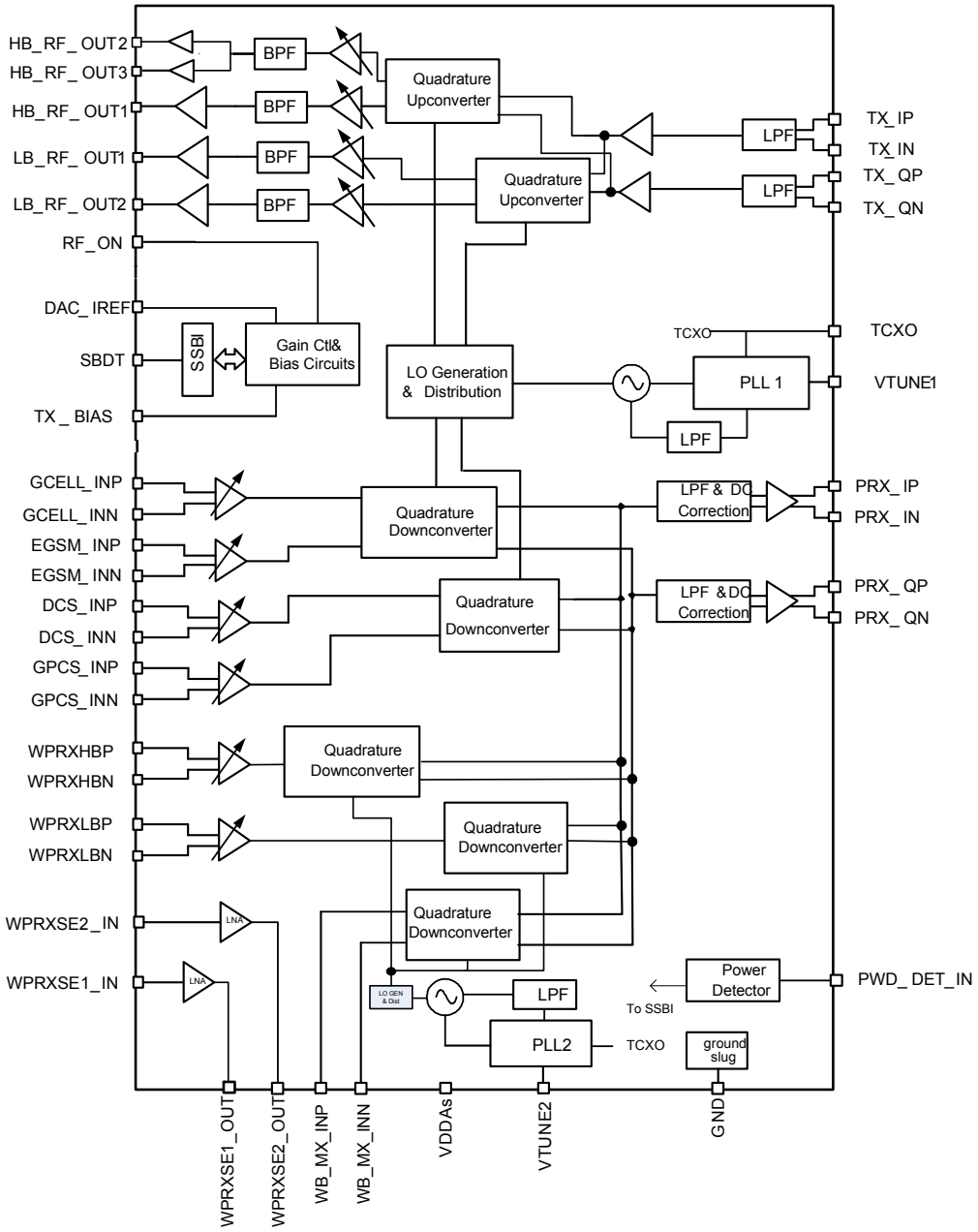


Figure 1-2 RTR6280 IC functional block diagram

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The RTR6285/RTR6280 IC supports multi-band, multi-mode phones.

- Receiver paths:
  - GSM/EDGE 850
  - GSM/EDGE 900
  - GSM/EDGE 1800
  - GSM/EDGE 1900
  - Two single-ended UMTS inputs
  - Two differential UMTS inputs
  - Three single-ended UMTS diversity inputs (RTR6285 only)
  - GPS receive (RTR6285 only)
- Transmitter paths:
  - Two low-band Tx paths for:
    - GSM/EDGE 850
    - GSM/EDGE 900
    - UMTS 800/850/900
  - Three high-band Tx paths for:
    - GSM/EDGE 1800
    - GSM/EDGE 1900
    - UMTS 1700/AWS/1800
    - UMTS 1900
    - UMTS 2100

Numerous secondary functions also are integrated on-chip:

- LNAs for UMTS Rx operation
- Quadrate demodulator to support UMTS Rx operation
- Three fractional-N synthesizers with on-chip VCOs and loop filters:
  - PLL1 and on-chip VCO support all transmitters of GSM 850/900/1800/1900 and UMTS low and high bands. It also serves all receivers of GSM 850/900/1800/1900.
  - PLL2 and on-chip VCO support primary and diversity receivers of UMTS high and low bands.
  - PLL3 and on-chip VCO support GPS receiver (RTR6285 only).

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- Transceiver LO generation and distribution circuits:
  - GSM/EDGE 850/900/1800/1900 Rx
  - GSM/EDGE 850/900/1800/1900 Tx
  - UMTS high and low bands primary and diversity Rx
  - UMTS high and low bands Tx
- Quadrature modulators to support GSM/GPRS/EDGE polar Tx and WCDMA/HSDPA Tx operations
- Integrated power detector
- Analog support functions
- Reference signal for the Mobile Station Modem™ (MSM™) device transmit DACs
- Transmit gain control
- Bias control
- Digital control circuits and interfaces
- Single-line serial bus interface (SSBI)
- Thermometer for temperature measurement

The device is fabricated using an advanced RF CMOS process that accommodates high-frequency, high-precision analog circuits and low-power CMOS functions. Designed to operate with low-voltage power supplies, it is compatible with single-cell Li-Ion batteries.

The RTR6285/RTR6280 IC is available in the 68-pin micro-quad flat no lead (68 mQFN) package that includes a large center ground slug for improved RF grounding, mechanical strength, and thermal continuity.

The RTR6285/RTR6280 ZIF architecture and highly integrated implementation minimizes handset PCB size and material cost. Major RTR6285/RTR6280 functional blocks are described in the following sections.

1.2.1 Primary receive signal paths

The RTR6285/RTR6280 receive paths include four GSM/EDGE Rx signal paths that support GSM 850, GSM 900, GSM 1800, and GSM 1900 bands and four WCDMA Rx signal paths (two single-ended and two differential) for one UMTS low-band and three UMTS high bands.

The quad-band GSM/EDGE Rx paths start from the handset front-end circuits (GSM Rx filters and antenna switch module). The four differential inputs are amplified with gain-stepped LNA circuits. Gain control is provided through software and serial interface. The LNA outputs drive the RF ports of quadrature RF-to-baseband downconverters. The downconverted baseband outputs are multiplexed and routed to lowpass filters (one I and one Q) whose passband and stopband characteristics supplement MSM device processing. These filter circuits allow DC offset corrections, and their differential outputs are buffered to interface with the MSM IC.

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The two RTR6285/RTR6280 UMTS single-ended inputs accept UMTS 2100/1900/1800/1700 input signals from the handset RF front-end filters. The UMTS Rx inputs are provided with on-chip LNAs that amplify the signal before second-stage filters that provide differential signals to a shared downconverter. This second-stage input is configured differentially to optimize second-order intermodulation and common mode rejection performance. The gain of the UMTS front-end amplifier and the UMTS second-stage differential amplifier is adjustable, under MSM control, to extend the dynamic range of the receivers.

The second-stage UMTS Rx amplifiers drive the RF ports of the quadrature RF-to-baseband downconverters. The downconverted UMTS Rx baseband outputs are routed to lowpass filters having passband and stopband characteristics suitable for UMTS Rx processing. These filter circuits allow DC offset corrections, and their differential outputs are buffered to an interface shared with GSM Rx to the MSM IC. The UMTS baseband outputs are turned off when the RTR6285/RTR6280 is downconverting GSM signals and turned on when the UMTS is operating.

The RTR6285/RTR6280 UMTS differential input paths stay on-chip; off-chip interstage filtering is not required. Other than this, the architecture is similar to the single-ended inputs.

1.2.2 Transmit signal paths

The RTR6285/RTR6280 transmit includes four transmit signal paths (two high bands and two low bands) supporting multi-bands and multi-modes GSM/GPRS/EDGE polar transmit and WCDMA/HSDPA transmit architectures.

The transmit path begins with differential baseband signals (I and Q) from the MSM device. These analog input signals are buffered, filtered by low-path filter, corrected for DC offsets, amplified, and then applied to the quadrature upconverter mixers.

The upconverter outputs are amplified by multiple variable gain stages that provide transmit AGC control. SSBI is used to do the gain control. The specified driver amplifier output level is achieved while supporting the GSM/EDGE and UMTS transmit standard's requirements for GSM ORFS, carrier and image suppression, WCDMA ACLR, spurious emissions, Rx-band noise, and so forth.

Again, the upconverter LO signals are generated by circuits discussed in Section 1.2.4. These upconverters translate the polar GMSK-modulated or 8-PSK modulated baseband PM signals and/or WCDMA baseband signals directly to the RF signals, which are filtered and feed into the GSM/EDGE polar PA and/or WCDMA PA. The WCDMA Tx power is coupled back to the RTR6285/RTR6280 internal power detector input pin, PWD_DET_IN, using a coupler for power measurement.

The low-band drive amplifiers are used to transmit the polar phase modulated (PM) signal for GSM/EDGE 850/900 while the high-band driver amplifiers are for the GSM/EDGE 1800/1900. By using the radioOne architecture, the same high-band transmit path can be used to transmit the UMTS 2100/1900/1800/1700 signal, and the low-band transmit path can be used to transmit the UMTS 800/850/900 signal, depending on the application.

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The envelope path is used in polar mode of operation for GSM and EDGE. Input from the MSM IC, the baseband envelope (AM) current signal is applied directly to the ramp control pin of the GSM/EDGE polar PA to modulate the power supply of the PA so that the polar-modulated GSM/EDGE signal in the MSM device can be recovered and transmitted.

1.2.3 Secondary WCDMA and GPS receive paths(RTR6285 only)

The three secondary WCDMA input paths stay on-chip; off-chip interstage filtering is not required. The three LNA outputs are routed to a single RF-to-baseband quadrature downconverter; again, only one LNA is active at a time. The GPS input path is followed by a dedicated downconverter. The GPS downconverter and secondary WCDMA downconverter outputs are multiplexed to drive a single set of baseband filter and buffer circuits. The secondary baseband output (in-phase and quadrature differential signals) is routed through the DRX_I/Q pins to the MSM device for further processing. This baseband interface supports WCDMA and GPS modes, whichever is active on the secondary path.

1.2.4 LO generation and distribution circuits

The integrated LO generation and distribution circuits are driven by internal VCOs to support various modes to yield highly flexible quadrature LO outputs that drive all GSM/EDGE, UMTS band and GPS upconverters and downconverters; with the help of these LO generation and distribution circuits, true ZIF architecture is employed in all GSM and UMTS band receivers and transmitters to translate the signal directly from RF to baseband and from baseband to RF.

Three fully functional fractional-N synthesizers, including VCOs and loop filters, are integrated within the RTR6285 IC while RTR6280 has two fractional-N synthesizers. The first synthesizer (PLL1) creates the transceiver LOs that support the UMTS transmitter, and all four GSM band receivers and transmitters including: GSM 850, GSM 900, GSM 1800, and GSM 1900. The second synthesizer (PLL2) provides the LO for the UMTS primary and secondary receivers (RTR6285 only). The third synthesizer (PLL3) provides the LO for the GPS receiver (RTR6285 only). An external TCXO input signal is required to provide the synthesizer frequency reference to which the PLL is phase- and frequency-locked. The RTR6285/RTR6280 IC integrates most of PLL loop filter components on-chip except three off-chip loop filter series capacitors, and significantly reduces off-chip component requirement. With the integrated fractional-N PLL synthesizers, the RTR6285/RTR6280 has the advantages of more flexible loop bandwidth control, fast lock time, and low-integrated phase error.

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1.2.5 Other integrated analog functions

The RTR6285/RTR6280 IC includes a single Tx analog baseband interface that is multiplexed between the transmitter paths to deliver the MSM IC output signal to the active path. The Tx baseband interface has four lines that are configured as two differential pairs – one pair for the in-phase component and one pair for the quadrature component. The Tx baseband interface is active during any single transmit mode (GSM, EDGE, WCDMA). The transmit baseband signals are generated by digital-to-analog converter (DAC) circuits within the MSM IC. Their performance is highly dependent upon the DAC reference signal, pin 67 (DAC_IREF), provided by the RTR6285/RTR6280 IC.

One external resistor set several RTR6285/RTR6280 IC internal operating currents (charge pump currents, signal path bias currents, and others). External resistors are required for pin 68 (TX_RBIAS) for bias control circuits; refer to the RF CMOS platform schematic for details.

1.2.6 Digital interfaces

Most control and status commands are communicated through the RTR6285/RTR6280 MSM device-compatible single-line serial bus interface (SSBI), enabling efficient initialization, WCDMA transmit gain control, control of device operating modes and parameters, verification of programmed parameters, and frequency lock status reports. The MSM device SSBI controller is the master while the RTR6285/RTR6280 IC is a slave.

The RTR6285/RTR6280 IC also provides a digital I/O pin for time-critical control signal:

- Pin 26: RF_ON – RF feature enable signal for UMTS transmitter ON; used as part of the power-up sequence in GSM mode.

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1.3 IC features

- Integral to the QUALCOMM MSM6260/MSM6255A/MSM6245™-series, MSM6280/6290™, MSM6246, MSM7225, QSD8650/QSD8250, and MSM7200A™-series chipset
- Multiband, multimode operation: UMTS 800/850/900, UMTS AWS/1700/1800/1900/2100, GSM/EDGE 850/900, and GSM/EDGE 1800/1900
- UMTS Diversity(RTR6285 only)
- GPS(RTR6285 only)
- GPRS/EDGE compliant
- Direct frequency conversions from analog baseband to RF and vice versa
- GSM 850, GSM 900, GSM 1800, and GSM 1900 receive signal path circuits
- UMTS receive signal path circuits
- GSM 850, GSM 900, GSM 1800, and GSM 1900 transmit signal path circuits
- UMTS transmit signal path circuits
- Dedicated ZIF RF-to-baseband quadrature downconverters
- Dedicated ZIF baseband-to-RF quadrature upconverters
- Dedicated gain-stepped LNA circuits
- RF AGC amplifiers, filter, and driver amplifier
- Dedicated gain control circuits
- Shared baseband lowpass filters, DC correction, and analog interface to the MSM
- Baseband interface from the MSM device with amplifiers and lowpass filters
- Baseband interface from the MSM device with amplifiers, DC correction, and lowpass filters
- Fully integrated fractional-N synthesizer PLL1, VCO, and loop filter components for GSM/EDGE Tx/Rx and UMTS Tx operations
- Fully integrated fractional-N synthesizer PLL2, VCO and loop filter components for UMTS Rx operation
- Fully integrated fractional-N synthesizer PLL3, VCO and loop filter components for GPS operation (RTR6285 only)
- Integrated LO generation and distribution circuits supporting multi-band and multi-mode operations
- Transmit power control range supports the UMTS standards
- Power reduction features via MSM device control extends handset talk-time and standby time
- Bias control circuits
- Integrated power detector
- Integrated thermometer

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- Single-line serial bus interface (SSBI)
- Selective circuit power-down
- Available in a small, thermally efficient package (68 pin mQFN)

Refer to the *RTR6285/RTR6280 RF Transceiver IC User Guide* (80-VD861-3) for more detailed descriptions of each RTR6285/RTR6280 function and control interface.

1.4 Terms and acronyms

A summary of terms and acronyms used within this document is provided for the reader's convenience.

Term or acronym	Definition
6285 series	The QUALCOMM chipset recommended for multi-modes, multi-bands for UMTS, GSM, and EDGE handsets
8-PSK	8-phase shift keying
ACLR	Adjacent channel leakage power ratio
AGC	Automatic gain control
AltCLR	Alternate channel leakage power ratio
AM-AM	Vamp to output amplitude characteristic of transmitter
AM-PM	Vamp to output phase characteristic of transmitter
API	Application programming interface
CP	Charge pump
DAC	Digital-to-analog converter
DSB	Double-side band
DS-WCDMA	Direct sequence WCDMA (referred to as UMTS 1900, UMTS 2100 in this document)
EDGE	Enhanced data rates for global evolution
GSM 850	GSM at 850 MHz band
GSM 900	EGSM at 900 MHz band
GSM 1800	DCS at 1800 MHz band
GSM 1900	GSM at 1900 MHz band
FAQ	Fast acquisition
GMSK	Gaussian minimum shift keying
GPRS	General packet radio service
GSM	Group Special Mobile or Global System for Mobile Communications
HSDPA	High-speed downlink packet access
IIP_2	Second order input intercept point
IIP_3	Third order input intercept point
Li	Lithium

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Term or acronym	Definition
LNA	Low-noise amplifier
LO	Local oscillator
MSM	Mobile Station Modem
P_1 dB desense	Power of blocker for 1 dB desense sensitivity
PA	Power amplifier
PAR	Peak-to-average ratio
PCB	Printed circuit board
PDM	Pulse density modulation
PLL	Phase-locked loop
PM	Power management
QFN	Quad flat no lead
radioOne	The QUALCOMM brand chipset that implements a ZIF radio architecture
RFL	Radio frequency LNA
RFR	Radio frequency receiver
RTR	Radio frequency transceiver
SSBI	Single-wired serial bus interface
SiGe	Silicon germanium
UMTS, UMTS 1900	Universal Mobile Telecommunications System at 1900 MHz
UMTS, UMTS 2100	Universal Mobile Telecommunications System at 2100 MHz
UMTS AWS	Universal Mobile Telecommunications System, Advanced Wirless Services
VCO	Voltage-controlled oscillator
VCTCXO	Voltage-controlled temperature-compensated crystal oscillator. Referred to as TCXO in this document.
WCDMA	Wideband CDMA (referred to as UMTS 1900, UMTS 2100 in this document)
Zero-IF	A radio architecture that converts received signals directly from RF to baseband and baseband to RF, eliminating the intermediate frequency (IF).
ZIF	Zero-IF

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2 Pin Definitions

The RTR6285/RTR6280 IC is available in the 68 mQFN package that includes a large center ground slug for electrical grounding, mechanical strength, and thermal continuity. Pin assignments are illustrated (Figure 2-1 and Figure 2-2) and defined (Table 2-1 and Table 2-2) in this chapter.

2.1 Pin assignments

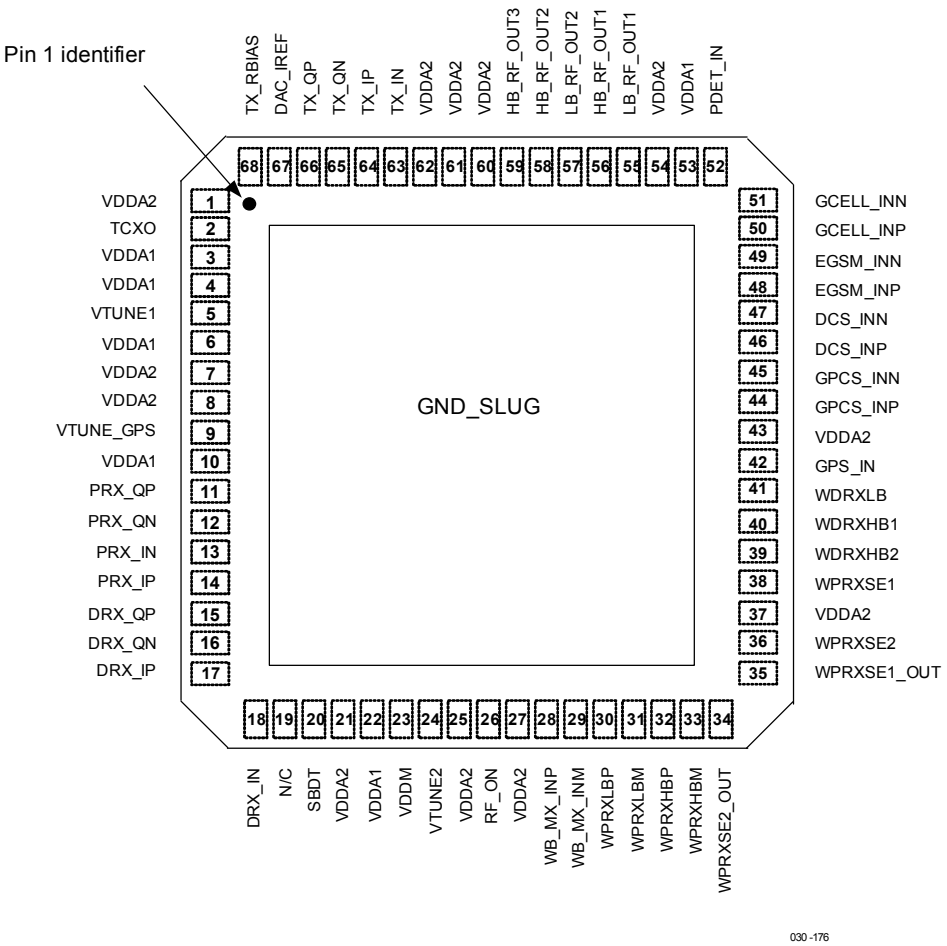


Figure 2-1 RTR6285 IC pin assignments (top view)

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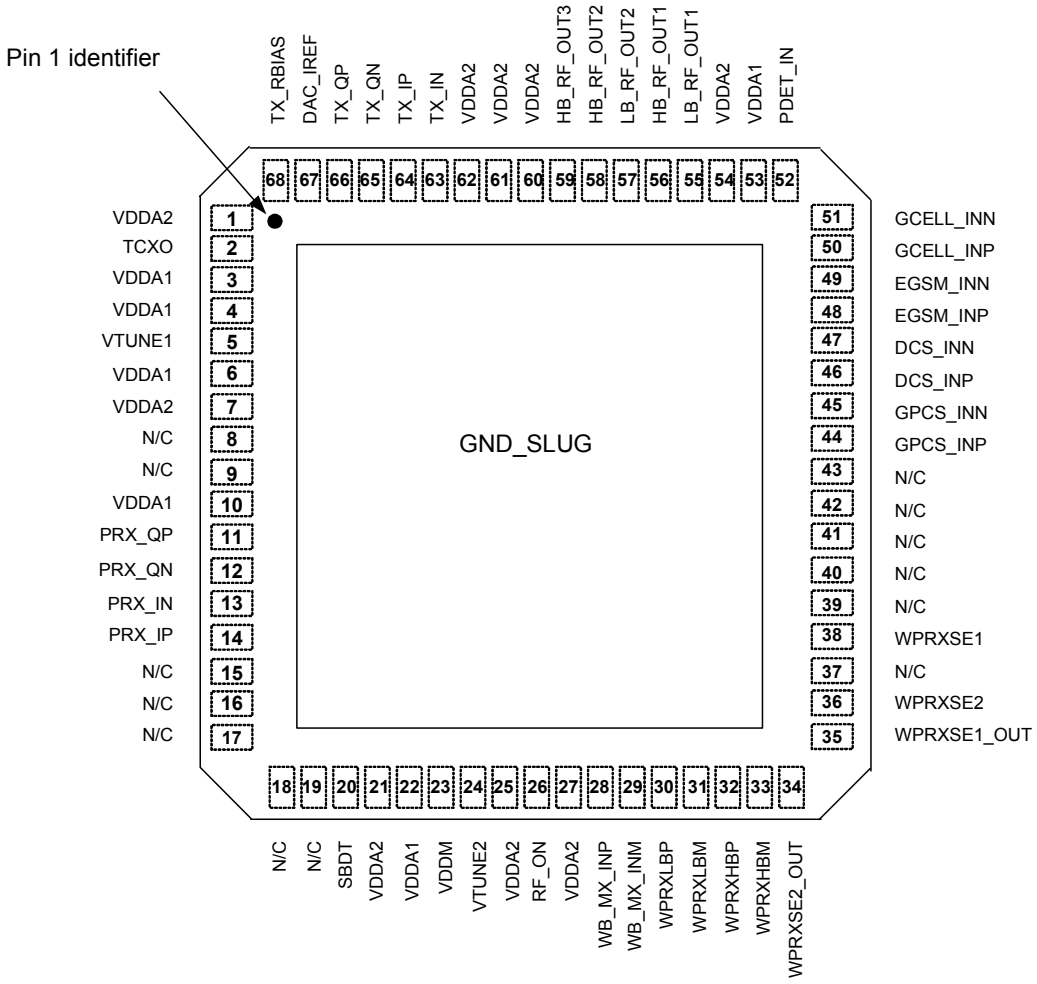


Figure 2-2 RTR6280 IC pin assignments (top view)

NOTE The center slug must be soldered directly to the PCB RF ground plane.

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2.2 Pin descriptions

Table 2-1 RTR6285 IC pin descriptions

Pin number	Pin name for RTR6285/RTR6280 IC	Type	Pin description
1	VDDA2	P	Analog power supply
2	TCXO	AI	TCXO signal input, 19.2 MHz
3	VDDA1	P	Analog power supply
4	VDDA1	P	Analog power supply
5	VTUNE1	AO	PLL1 off-chip loop filter series cap
6	VDDA1	P	Analog power supply
7	VDDA2	P	Analog power supply
8	VDDA2	P	Analog power supply
9	VTUNE_GPS	AO	GPS off-chip loop filter series cap
10	VDDA1	P	Analog power supply
11	PRX_QP	AO	Primary path Rx Q positive output
12	PRX_QN	AO	Primary path Rx Q negative output
13	PRX_IN	AO	Primary path Rx I negative output
14	PRX_IP	AO	Primary path Rx I positive output
15	DRX_QP	AO	Diversity/GPS path Rx Q positive output
16	DRX _QN	AO	Diversity/GPS path Rx Q negative output
17	DRX _IP	AO	Diversity/GPS path Rx I positive output
18	DRX_IN	AO	Diversity/GPS path Rx I negative output
19	N/C	DNC	Not connected
20	SBDT	IO	SSBI data digital CMOS input and output.
21	VDDA2	P	Analog power supply
22	VDDA1	P	Analog power supply
23	VDDM	P	MSM digital I/O power supply voltage. Connect to the MSM PAD VDD voltage.
24	VTUNE2	AO	PLL2 off-chip loop filter series cap
25	VDDA2	P	Analog power supply
26	RF ON	DI	RF enable signal, used for enabling WCDMA Tx, and used as part of power-up sequence in GSM modes
27	VDDA2	P	Analog power supply
28	WB_MX_INP	AI	WCDMA mixer positive input
29	WB_MX_INM	AI	WCDMA mixer negative input
30	WPRXLBP	AI	WCDMA primary Rx low-band LNA input for differential duplexer path positive input
31	WPRXLBM	AI	WCDMA primary Rx low-band LNA input for differential duplexer path negative input

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Table 2-1 RTR6285 IC pin descriptions (continued)

Pin number	Pin name for RTR6285/RTR6280 IC	Type	Pin description
32	WPRXHBP	AI	WCDMA primary Rx high-band LNA input for differential duplexer path positive input
33	WPRXHBM	AI	WCDMA primary Rx high-band LNA input for differential duplexer path negative input
34	WPRXSE2_OUT	AO	WCDMA primary Rx single-ended LNA output
35	WPRXSE1_OUT	AO	WCDMA primary Rx single-ended LNA output
36	WPRXSE2	AI	WCDMA primary Rx single-ended LNA input
37	VDDA2	P	Analog power supply
38	WPRXSE1	AI	WCDMA primary Rx single-ended LNA input
39	WDRXHB2	AI	WCDMA diversity high-band single-ended LNA input
40	WDRXHB1	AI	WCDMA diversity high-band single-ended LNA input
41	WDRXLB	AI	WCDMA diversity low-band single-ended LNA input
42	GPS_IN	AI	GPS Rx LNA input
43	VDDA2	P	Analog power supply
44	GPCS_INP	AI	GSM PCS Rx LNA positive input
45	GPCS_INN	AI	GSM PCS Rx LNA negative input
46	DCS_INP	AI	GSM Rx high-band LNA positive input
47	DCS_INN	AI	GSM Rx high-band LNA negative input
48	EGSM_INP	AI	GSM Rx low-band LNA positive input
49	EGSM_INN	AI	GSM Rx low-band LNA negative input
50	GCELL_INP	AI	GSM Rx low-band LNA positive input
51	GCELL_INN	AI	GSM Rx low-band LNA negative input
52	PDET_IN	AI	Power detector input pin
53	VDDA1	P	Analog power supply
54	VDDA2	P	Analog power supply
55	LB_RF_OUT1	AO	1st low-band drive amp RF output. Used for GSM.
56	HB_RF_OUT1	AO	1st high-band drive amp RF output. Used for GSM.
57	LB_RF_OUT2	AO	2nd low-band drive amp RF output. Used for WCDMA.
58	HB_RF_OUT2	AO	2nd high-band drive amp RF output. Used for WCDMA.
59	HB_RF_OUT3	AO	3rd high-band drive amp RF output. Used for WCDMA.
60	VDDA2	P	Analog power supply
61	VDDA2	P	Analog power supply
62	VDDA2	P	Analog power supply
63	TX_IN	AI	TX_I negative input
64	TX_IP	AI	TX I positive input
65	TX_QN	AI	TX Q negative input

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Table 2-1 RTR6285 IC pin descriptions (continued)

Pin number	Pin name for RTR6285/RTR6280 IC	Type	Pin description
66	TX_QP	AI	TX Q positive input
67	DAC_IREF	AO	MSM Tx DAC reference current, current source output
68	TX_RBIAS	AI	Bias current setting resistor
--	Gnd slug		Global ground for the chip

Table 2-2 RTR6280 IC pin descriptions

Pin number	Pin name for RTR6285/RTR6280 IC	Type	Pin description
1	VDDA2	P	Analog power supply
2	TCXO	AI	TCXO signal input, 19.2 MHz
3	VDDA1	P	Analog power supply
4	VDDA1	P	Analog power supply
5	VTUNE1	AO	PLL1 off-chip loop filter series cap
6	VDDA1	P	Analog power supply
7	VDDA2	P	Analog power supply
8	N/C	DNC	Not connected
9	N/C	DNC	Not connected
10	VDDA1	P	Analog power supply
11	PRX_QP	AO	Primary path Rx Q positive output
12	PRX_QN	AO	Primary path Rx Q negative output
13	PRX_IN	AO	Primary path Rx I negative output
14	PRX_IP	AO	Primary path Rx I positive output
15	N/C	DNC	Not connected
16	N/C	DNC	Not connected
17	N/C	DNC	Not connected
18	N/C	DNC	Not connected
19	N/C	DNC	Not connected
20	SBDT	IO	SSBI data digital CMOS input and output.
21	VDDA2	P	Analog power supply
22	VDDA1	P	Analog power supply
23	VDDM	P	MSM digital I/O power supply voltage. Connect to the MSM PAD VDD voltage.
24	VTUNE2	AO	PLL2 off-chip loop filter series cap
25	VDDA2	P	Analog power supply

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Table 2-2 RTR6280 IC pin descriptions (continued)

Pin number	Pin name for RTR6285/RTR6280 IC	Type	Pin description
26	RF ON	DI	RF enable signal, used for enabling WCDMA Tx, and used as part of power-up sequence in GSM modes
27	VDDA2	P	Analog power supply
28	WB_MX_INP	AI	WCDMA mixer positive input
29	WB_MX_INM	AI	WCDMA mixer negative input
30	WPRXLBP	AI	WCDMA primary Rx low-band LNA input for differential duplexer path positive input
31	WPRXLBM	AI	WCDMA primary Rx low-band LNA input for differential duplexer path negative input
32	WPRXHBP	AI	WCDMA primary Rx high-band LNA input for differential duplexer path positive input
33	WPRXHBM	AI	WCDMA primary Rx high-band LNA input for differential duplexer path negative input
34	WPRXSE2_OUT	AO	WCDMA primary Rx single-ended LNA output
35	WPRXSE1_OUT	AO	WCDMA primary Rx single-ended LNA output
36	WPRXSE2	AI	WCDMA primary Rx single-ended LNA input
37	N/C	DNC	Not connected
38	WPRXSE1	AI	WCDMA primary Rx single-ended LNA input
39	N/C	DNC	Not connected
40	N/C	DNC	Not connected
41	N/C	DNC	Not connected
42	N/C	DNC	Not connected
43	N/C	DNC	Not connected
44	GPCS_INP	AI	GSM PCS Rx LNA positive input
45	GPCS_INN	AI	GSM PCS Rx LNA negative input
46	DCS_INP	AI	GSM Rx high-band LNA positive input
47	DCS_INN	AI	GSM Rx high-band LNA negative input
48	EGSM_INP	AI	GSM Rx low-band LNA positive input
49	EGSM_INN	AI	GSM Rx low-band LNA negative input
50	GCELL_INP	AI	GSM Rx low-band LNA positive input
51	GCELL_INN	AI	GSM Rx low-band LNA negative input
52	PDET_IN	AI	Power detector input pin
53	VDDA1	P	Analog power supply
54	VDDA2	P	Analog power supply
55	LB_RF_OUT1	AO	1st low-band drive amp RF output. Used for GSM.
56	HB_RF_OUT1	AO	1st high-band drive amp RF output. Used for GSM.
57	LB_RF_OUT2	AO	2nd low-band drive amp RF output. Used for WCDMA.

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Table 2-2 RTR6280 IC pin descriptions (continued)

Pin number	Pin name for RTR6285/RTR6280 IC	Type	Pin description
58	HB_RF_OUT2	AO	2nd high-band drive amp RF output. Used for WCDMA.
59	HB_RF_OUT3	AO	3rd high-band drive amp RF output. Used for WCDMA.
60	VDDA2	P	Analog power supply
61	VDDA2	P	Analog power supply
62	VDDA2	P	Analog power supply
63	TX_IN	AI	TX_I negative input
64	TX_IP	AI	TX I positive input
65	TX_QN	AI	TX Q negative input
66	TX_QP	AI	TX Q positive input
67	DAC_IREF	AO	MSM Tx DAC reference current, current source output
68	TX_RBIAS	AI	Bias current setting resistor
	Gnd slug		Global ground for the chip

Notes:

Type definitions:

- AI = Analog input
- AO = Analog output
- DI = Digital input from MSM device
- DNC = Do not connect
- DO = Digital output to MSM device
- P = Power or ground

VDDA1s are connected to 2.7 V (nominal) supply.

VDDA2s are connected to 2.1 V (nominal) supply.

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3 Electrical Specifications

3.1 Absolute maximum ratings

Operating the RTR6285/6280 IC under conditions beyond its absolute maximum ratings (Table 3-1) may damage the device. Absolute maximum ratings are limiting values to be considered individually when all other parameters are within their specified operating range. Functional operation and specification compliance under any absolute maximum rating condition, or after exposure to any of these conditions, is not guaranteed or implied. Exposure may affect the device reliability.

Table 3-1 Absolute maximum ratings

Parameter		Rating
V_{DDA}, V_{DDM}	Power supply voltage	-0.5 to 3.2 V
V_{IN}	Voltage applied to any input or output pin (see note)	-0.5 V to V_{DDX} V
Input power level	Maximum survival LNA input power level	0 dBm
T_S	Storage temperature	-55°C to +150°C
t_{sc}	Short circuit duration to GND or V_{DD}	1 sec
V_{HBM}	Electrostatic discharge rating, human body model	1500 V
V_{CDM}	Electrostatic discharge rating, charge device model	200 V

Note: V_{DDX} is the supply voltage associated with the input or output pin to which the test voltage is applied.

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3.2 Recommended operating conditions

Operating conditions include parameters that are under the control of the user: power supply voltage and ambient temperature (Table 3-2). The RTR6285/6280 IC meets all performance specifications listed in Section 3.3 through Section 3.8 and their subsections when used within the recommended operating conditions unless otherwise noted in those sections (provided the absolute maximum ratings have never been exceeded).

Table 3-2 Recommended operating conditions

Parameter		Min	Typ	Max	Units
V_{DDA1}	Supply voltage, analog circuits	2.62	2.7	2.78	V
V_{DDA2}	Supply voltage, analog circuits	2.03	2.1	2.17	V
V_{DDM}	Supply voltage, I/O circuits		2.6		V
T_C	Case operating temperature	-20	+25	+85	°C

Notes:
Analog supply pins (V_{DDA}) may be powered down while the digital I/O supply pin (V_{DDM}) is powered up.

3.3 Power supply and digital logic characteristics

This section includes physical characteristics such as I/O capacitance and DC characteristics such as digital I/O levels and power supply currents (Table 3-3). Supply currents are based on RTR6285/6280 IC operation at room temperature (+25°C) using default parameter settings and nominal supply voltages in Table 3-2. See the detail setting in Section 3.4.

Table 3-3 Current consumption

Parameters	Condition	2.1-V supply current (typical)	2.7-V supply current (typical)	Total supply current at battery [1]	Unit
Sleep current	All supplies are on; chip is turned off.	60	37	68	µA
GSM Rx current low band	Highest gain	11	91	81	mA
GSM Rx current high band	Highest gain	11	93	83	mA
GSM Tx current low band		70	83	112	mA
GSM Tx current high band		66	46	79	mA
UMTS IMT band SE Rx current	G0 gain mode G1 gain mode	59 53	4 4	41 37	mA
UMTS AWS band differential Rx current	G0 gain mode G1 gain mode	69 56	4 4	47 39	mA

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Table 3-3 Current consumption (continued)

Parameters	Condition	2.1-V supply current (typical)	2.7-V supply current (typical)	Total supply current at battery [1]	Unit
UMTS 800-band differential Rx current	G0 gain mode	71	4	48	mA
	G1 gain mode	52	4	36	
UMTS IMT band Tx current	@Rated output power	52	4	36	mA
	@-8 dBm output power	38	4	27	
UMTS AWS band Tx current	@Rated output power	52	4	36	mA
	@-8 dBm output power	37	4	27	
UMTS 800-band Tx current	@Rated output power	56	4	39	mA
	@-8 dBm output power	36	4	26	
UMTS DRx low-band current	G0 gain mode	38	0	24	mA
	G1 gain mode	32	0	20	
UMTS DRx high-band current	G0 gain mode	37	0	24	mA
	G1 gain mode	30	0	19	
GPS	Low power mode	41	4	29	mA
	High power mode	52	4	36	

[1] Assume 2.1-V and 2.7-V supply are using SMPS with 90% efficiency and battery voltage of 3.6 V.

Table 3-4 DC electrical characteristics

Parameter	Symbol	Condition	Minimum	Maximum	Units
Logic high-level input voltage	V_{IH}		$0.65*V_{DDd}$		V
Logic low-level input voltage	V_{IL}			$0.35* V_{DDd}$	V
Logic high-level output voltage	V_{OH}	V_{DD} = Minimum	$V_{DDd} – 0.45$		V
Logic low-level output voltage	V_{OL}	V_{DD} = Maximum		0.45	V
Logic input leakage current	I_L	V_{DD} = Maximum V_{in} = GND to V_{DD}	-100	+100	nA
Input capacitance (digital inputs)	C_{in-d}			5	pF
Load capacitance (digital outputs)	C_{l-d}			15	pF
Logic low-level output current	I_{OL}			-6	mA
Logic high-level output current	I_{OH}		6		mA

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3.4 GSM/EDGE receive specifications

The RTR6285/6280 IC includes four receive signal paths: GSM 850, GSM 900, GSM 1800, and GSM 1900. Specifications for all paths are presented in the following sections.

3.4.1 GSM 850/900 receive signal path

The GSM 850 and GSM 900 receive signal path specifications in this subsection are based on the test input described in the notes following Table 3-5. This test input allows measurements using standard 50-ohm single-ended test equipment even though the RTR6285/6280 IC requires a differential signal at the GSM 850 input (pins 50 and 51). Handset implementations are expected to accomplish this single-ended to differential transformation using a SAW filter; the filter, matching components; and PCB traces must provide adequate amplitude and phase balance (≤ 1 dB and ≤ 5 degrees, respectively).

Table 3-5 GSM 850/900 receive signal path specifications

Parameter	Comments	Min	Typ	Max	Unit	Notes
RF input						
Input frequency range	GSM 850 band, downlink	869		894	MHz	
	GSM 900 band, downlink	925		960	MHz	
Input VSWR	Based on 100-ohm differential source impedance; includes matching network.			2:1		
LO generation and distribution – see Section 3.8						
RF-to-baseband signal path (valid for all gain modes unless noted otherwise)						
Gain variation	Over frequency range Over temperature	-1.25 -0.3		1.25 0.3	dB dB	
Survivable input level		0			dBm	
Residual sideband level	Due to amplitude and phase imbalance	29	44		dB	
Residual output DC		-80		80	mV	
LO to RF leakage	Differential, in RF channel, at LNA input			-79	dBm	
Gain mode 0						
Gain		68	72.5	77	dB	2
Noise figure	Double sideband		2.8	4.5	dB	6
P1 dB desense (in band)	In-band signal = -101 dBm	-65	-60		dBm	
P1 dB desense (blocking @ 3 MHz offset)		-25			dBm	3
Input IP_3		-17	-15		dBm	4
Input IP_2	In-band tone power = -101 dBm	40	50		dBm	5
Gain mode 1						
Gain		54	58.5	63	dB	2
Noise figure	Double sideband		3.2	4.9	dB	6
P1 dB desense (in band)		-60	-55		dBm	

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Table 3-5 GSM 850/900 receive signal path specifications (continued)

Parameter	Comments	Min	Typ	Max	Unit	Notes
Gain mode 2						
Gain		36.5	41	45.5	dB	2
Noise figure	Double sideband			7.0	dB	6
P1 dB desense (in band)		-43	-38		dBm	
Gain mode 3						
Gain		24.5	29	33.5	dB	2
Noise figure	Double sideband			30	dB	6
P1 dB desense (in band)		-26.6	-21.6		dBm	
Gain mode 4						
Gain		7	11.5	16	dB	2
Noise figure	Double sideband			35	dB	6
P1 dB desense (in band)		-26.6	-21.6		dBm	

Notes:

1. The analog baseband output pins from RTR6285/6280 are connected to the MSM ICs. Individual trace and load capacitance should not to exceed 15 pF on the I or Q lines to the MSM. The I and Q load resistance and capacitance should be equal.
2. Gain values are voltage conversion gains.
3. Out-of-band jammer (blocker) input power that reduces the in-band output signal power by 1 dB.
4. Test conditions for third-order input intercept point measurements: CW input jammer level = -49 dBm at 800 kHz offset, CW input jammer level = -49 dBm at 1650 kHz offset.
5. Test conditions for in-band second-order input intercept point measurements: CW input jammer #1 level = -33 dBm at 6000 kHz offset, CW input jammer #2 level = -33 dBm at 6050 kHz offset.
6. Noise figure must be met for 2:1 source VSWR in a 100-ohm system. Noise figure or output noise voltage is integrated from 100 Hz to 100 kHz.
7. Performance specifications are based on measurements taken using a hybrid power splitter to create two 50-ohm outputs that are 180 degrees out-of-phase (Figure 3-1). The result is a 100-ohm differential input to the test board connected by two coaxial cables, with calibrated traces to the RTR6285/6280 input and its matching components. The matching circuit for IC-level testing is different than recommended handset designs. See the *RTR6285/6280 Device User Guide* for recommendations. Performance specifications listed in the table include the matching networks but not the hybrid splitter, coaxial cables, or calibrated PCB traces.

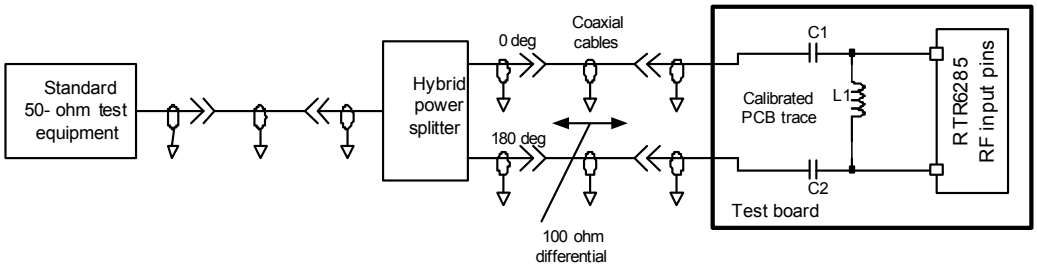


Figure 3-1 RF input test setup

3.4.2 GSM 1800/1900 receive signal path

The GSM1800 receive signal path specifications given in this subsection are based on the test input described in the Table 3-6 notes. This test input allows measurements using standard 50-ohm single-ended test equipment even though the RTR6285/6280 IC requires a differential signal at the GSM 1800 input (pins 36 and 37). Handset implementations are

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expected to accomplish this single-ended to differential transformation using a SAW filter; the filter, matching components, and PCB traces must provide adequate amplitude and phase balance (≤ 1.5 dB and ≤ 15 degrees, respectively).

Table 3-6 GSM 1800/1900 receive signal path specifications

Parameter	Comments	Min	Typ	Max	Unit	Notes
RF input						
Input frequency range	GSM1800 band, downlink	1805		1880	MHz	
	GSM1900 band, downlink	1930		1990	MHz	
Input VSWR	Based on 100-ohm differential source impedance; includes matching network.			2:1		
LO generation and distribution – see Section 3.8						
RF-to-baseband signal path (valid for all gain modes unless noted otherwise)						
Gain variation	Over frequency range Over temperature	-1.25 -0.3		+1.25 +0.3	dB dB	
Survivable input level		0			dBm	
Residual sideband level	Due to amplitude and phase imbalance	30	40		dB	
Residual output DC		-80		80	mV	
LO to RF leakage	Differential, in RF channel, at LNA input			-79	dBm	
Gain mode 0						
Gain		69.5	74	78.5	dB	2
Noise figure	Double sideband		3.0	5.0	dB	6
P1 dB desense (in band)		-65	-60		dBm	
P1 dB desense (blocking @ 3 MHz offset)	In-band signal = -99 dBm	-26			dBm	3
Input IP_3		-17	-15		dBm	4
Input IP_2	In-band tone power = -101 dBm	40	48		dBm	5
Gain mode 1						
Gain		53.5	58	62.5	dB	2
Noise figure	Double sideband		3.4	5.4	dB	6
P1 dB desense (in band)		-60	-55		dBm	
Gain mode 2						
Gain		37.5	42	46.5	dB	2
Noise figure	Double sideband			7.0	dB	6
P1 dB desense (in band)		-43	-38		dBm	
Gain mode 3						
Gain		22	26.5	31	dB	2
Noise figure	Double sideband			30	dB	6
P1 dB desense (in band)		-26.6	-21.6		dBm	
Gain mode 4						

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Table 3-6 GSM 1800/1900 receive signal path specifications (continued)

Parameter	Comments	Min	Typ	Max	Unit	Notes
Gain		6	10.5	15	dB	2
Noise figure	Double sideband			35	dB	6
P1 dB desense (in band)		-26.6	-21.6		dBm	

Notes:

1. The analog baseband output pins from RTR6285/6280 are connected to the MSM ICs. Individual trace and load capacitance should not to exceed 15 pF on the I or Q lines to the MSM/RFR. The I and Q load resistance and capacitance should be equal.
2. Gain values are voltage conversion gains.
3. Out-of-band jammer (blocker) input power that reduces the in-band output signal power by 1 dB.
4. Test conditions for third-order input intercept point measurements: CW input jammer level = -49 dBm at 800 kHz offset, CW input jammer level = -49 dBm at 1650 kHz offset.
5. Test conditions for in-band second-order input intercept point measurements: CW input jammer #1 level = -33 dBm at 6000 kHz offset, CW input jammer #2 level = -33 dBm at 6050 kHz offset.
6. Noise figure must be met for 2:1 source VSWR in a 100-ohm system. Noise figure or output noise voltage is integrated from 100 Hz to 100 kHz.
7. Performance specifications are based on measurements taken using a hybrid power splitter to create two 50-ohm outputs that are 180 degrees out-of-phase (Figure 3-1). The result is a 100-ohm differential input to the test board connected by two coaxial cables, with calibrated traces to the RTR6285/6280 input and its matching components. The matching circuit for IC-level testing is different than recommended handset designs. See *RTR6285/6280 Device User Guide* for recommendations. Performance specifications listed in the table include the matching networks but not the hybrid splitter, coaxial cables, or calibrated PCB traces.

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3.5 GSM/EDGE transmit signal path specifications

The RTR6285/6280 IC includes significant circuits for supporting GSM/EDGE polar transmit signal paths, which include low-band path for GSM 850 and GSM 900, and high-band path for GSM 1800 and GSM 1900. The baseband I/Q signals from MSM are directly upconverted to RF frequency using ZIF architecture. Specifications for each set of transmitter circuits are given in the following sections.

3.5.1 GSM 850/900 transmit signal paths

Table 3-7 GSM 850/900 (low-band) signal path specifications

Specification	Comments	Min	Nom	Max	Units	Notes
Operating frequency	GSM 850 band	824		849	MHz	
	GSM 900 band	880		915	MHz	
Output power			14		dBm	1
Output power variation	Over temperature	-1		+1	dB	
Sideband suppression	67.7 kHz CW I & Q (quadrature) sine wave input		-45	-35	dBc	1
Carrier suppression	67.7 kHz CW I & Q (quadrature) sine wave input		-37	-33	dBc	1
Output spectrum	PN 9 GMSK modulation					1, 2
200 kHz (30 kHz RBW)			-36	-33	dBc	
250 kHz (30 kHz RBW)			-42	-36	dBc	
400 kHz (30 kHz RBW)			-66	-63	dBc	
1.8 MHz (100 kHz RBW)				-68	dBc	
3 MHz (100 kHz RBW)				-70	dBc	
6 MHz (100 kHz RBW)				-76	dBc	
Output noise	Include the LO phase noise					1
10 MHz offset				-153	dBc/Hz	
20 MHz offset				-163.5	dBc/Hz	
Spurs at output in Rx band greater than -112 dBc	LB, output spurs no more than five cases			-90	dBc	
RMS phase error			1	2	Degree	1

Notes:

1. Measured low-band RF outputs.
2. For output spectrum measurement, these requirements are in dBc relative to a measurement in 30 kHz on the carrier using the specified resolution bandwidth.

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3.5.2 GSM 1800/1900 transmit signal paths

Table 3-8 GSM 1800/1900 (high-band) signal path specifications

Specification	Comments	Min	Nom	Max	Units	Note
Operating frequency	GSM1800	1710		1785	MHz	
	GSM1900	1850		1910	MHz	
Output power			11		dBm	1
Output power variation	Over temperature	-1.5		+1.5	dB	
Sideband suppression	67.7 kHz CW I & Q (quadrature) sine wave input		-40	-35	dBc	1
Carrier suppression	67.7 kHz CW I & Q (quadrature) sine wave input - w/ CS cal		 -40	 -35	 dBc	1
Output spectrum 200 kHz (30 kHz RBW) 250 kHz (30 kHz RBW) 400 kHz (30 kHz RBW) 1.8 MHz (100 kHz RBW) 3 MHz (100 kHz RBW) 6 MHz (100 kHz RBW)	PN 9 GMSK modulation		 -36 -43 -66	 -33 -36 -63 -68 -70 -76	 dBc dBc dBc dBc dBc dBc	1, 2
Output noise 10 MHz offset 20 MHz offset	Include the LO phase noise and fractional spurs			 -150 -155	 dBc/Hz dBc/Hz	1
Spurs at output in Rx band greater than -112 dBc	HB, output spurs no more than 5 cases		-90		dBc	
RMS phase error			2.0	3.5	Degree	1

Notes:

1. Measured high-band RF outputs.
2. For output spectrum measurement, these requirements are in dBc relative to a measurement in 30 kHz on the carrier using the specified resolution bandwidth.

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3.6 WCDMA primary receive signal path specifications

3.6.1 WCDMA balanced high-band primary receive specifications

Table 3-9 WCDMA balanced high-band primary receive specifications

Specification	Comments	Min	Typ	Max	Units
RF input frequency range	UMTS AWS band UMTS PCS band	2110 1930		2155 1990	MHz
RF input impedance	Differential		100		Ohms
Input return loss	All gain states	10			dB
Gain mode 0	G0				
Voltage conversion gain		53	57	61	dB
Noise figure	Small signal		3.0	5	dB
Input IP3	Jammers 1 and 2 at -44 dBm	-18	-14.6		dBm
Input IP2	with calibration	55			dBm
Gain mode 1	G1				
Voltage conversion gain		42	46	50	dB
Noise figure			13.5	16	dB
Input IP3	Jammers 1 and 2 at -28 dBm	-3	-6.5		dBm
Input IP2		40			dBm
Gain mode 2	G2				
Voltage conversion gain		30	34	38	dB
Noise figure				25	dB
Input IP3	Use jammers 5 and 6	-24			dBm
Gain mode 3	G3				
Voltage conversion gain		17			dB
Noise figure	DSB			33	dB
Input IP3	Use jammers 5 and 6	-13			dBm
Gain mode 4	G4				
Voltage conversion gain		4			dB
Noise figure	DSB			43	dB
Input IP3	Use jammers 5 and 6	-4.5			dBm

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3.6.2 WCDMA balanced low-band primary receive specifications

Table 3-10 WCDMA balanced low-band primary receive specifications

Specification	Comments	Min	Typ	Max	Units
RF input frequency range	UMTS cell band	869		894	MHz
	UMTS 900 band	925		960	MHz
RF input impedance	Differential		100		Ohms
Input return loss	All gain states	10			dB
Gain mode 0	G0				
Voltage conversion gain		53	57	61	dB
Noise figure	Small signal		2.8	4.5	dB
Input IP3	Jammers 1 and 2 at -44 dBm	-15	-11		dBm
Input IP2	with calibration	55			dBm
Gain mode 1	G1				
Voltage conversion gain		40	44	48	dB
Noise figure			13	17	dB
Input IP3	Jammers 1 and 2 at -28 dBm	-7	-3.5		dBm
Input IP2		40			dBm
Gain mode 2	G2				
Voltage conversion gain		28	32	36	dB
Noise figure			22.5	25	dB
Input IP3	Use jammers 5 and 6	-22			dBm
Gain mode 3	G3				
Voltage conversion gain		17			dB
Noise figure	DSB			33	dB
Input IP3	Use jammers 5 and 6	-13			dBm
Gain mode 4	G4				
Voltage conversion gain		4			dB
Noise figure	DSB			43	dB
Input IP3	Use jammers 5 and 6	-4.5			dBm

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3.6.3 WCDMA unbalanced primary receive specifications (high bands only)

Table 3-11 WCDMA unbalanced primary Rx specification – high bands only

Specification	Comments	Min	Typ	Max	Units
RF input frequency range	UMTS 2100 band	2110		2170	MHz
	UMTS 1900 band	1930		1990	MHz
	UMTS 1700 band	1844.9		1879.9	MHz
LNA gain mode 0	G0				
Input return loss	50 ohms w/external match	10			dB
Output return loss	50 ohms w/external match	10			dB
Power gain		14.5	17	19.5	dB
Noise figure	Small signal		1.5	2.3	dB
Input IP3	Jammers 1 and 2 at -30 dBm	-5	0		dBm
LNA gain mode 1	G1				
Input return loss	50 ohms w/external match	8			dB
Output return loss	50 ohms w/external match	8			dB
Power gain		-7	-5	-3	dB
Noise figure			5.5	8	dB
Input IP3	Jammers 1 and 2 at -20 dBm	0			dBm
LNA gain mode 2	G2				
Input return loss	50 ohms w/external match	10			dB
Output return loss	50 ohms w/external match	10			dB
Power gain		-22.5	-20	-17.5	dB
Noise figure				25	dB
Input IP3	Jammers 1 and 2 at -12 dBm	0			dBm
Mixer high-gain mode					
Input VSWR	100-ohm differential, external match			2:1	
Voltage conversion gain		40.5	43	45.5	dB
Noise figure	Double side band		12.5	14	dB
Input IP3	IMT band: jammers 1 and 2 at -30 dBm; in-band tone at -86 dBm	-2			dBm
	PCS and 1700 band: jammers 1 and 2 at -30 dBm, in-band tone at -81 dBm	0			dBm
Input IP2	Jammers 3 and 4 at -28 dBm; in-band tone at -86 dBm	43			dBm

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Table 3-11 WCDMA unbalanced primary Rx specification – high bands only (continued)

Specification	Comments	Min	Typ	Max	Units
Mixer low-gain mode					
Input VSWR	100-ohm differential, external match			2:1	
Voltage conversion gain		25.5	28	30.5	dB
Noise figure	Double side band		25	27	dB
Input IP3	Jammers 1 and 2 at -32 dBm; in-band tone at -60 dBm	-5	5		dBm

Notes: The test frequencies are listed below:

Band	In-band RF	1	2	3	4
Cell low	871.5	867.9	865.5	861.4	861.2
Cell high	891.5	895.1	897.5	901.6	901.8
EGSM low	927.5	923.9	921.5	917.4	917.2
EGSM high	957.5	961.1	963.5	967.6	967.8
DCS low	1807.5	1803.9	1801.5	1817.4	1817.6
DCS high	1877.5	1881.1	1883.5	1867.6	1867.4
PCS low	1932.5	1928.9	1926.5	1942.4	1942.6
PCS high	1987.5	1991.1	1993.5	1977.6	1977.4
IMT low	2112.5	2108.9	2106.5	2122.4	2122.6
IMT high	2167.5	2171.1	2173.5	2157.6	2157.4

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3.7 WCDMA transmit signal path specifications

The RTR6285/6280 WCDMA transmit paths share the same transmit paths as GSM and support multi-transmit modes: UMTS 2100, UMTS 1900, and UMTS 1800 on high-band transmit drivers, and UMTS 800 and UMTS 850 on low-band transmit drivers.

3.7.1 UMTS high-band transmit signal path

Table 3-12 UMTS high-band Tx specifications

Parameter	Comments	Min	Typ	Max	Unit	Notes
RF output						
Output frequency range	UMTS 2100 UMTS 1900 UMTS 1700 UMTS AWS	1920 1850 1749.9 1710		1980 1910 1784.9 1755	MHz MHz MHz MHz	
Maximum output power (average channel power)	UMTS 2100 band UMTS 1900 UMTS 1700/AWS	6.5 7 6.5	7 8 8		dBm dBm dBm	5
Minimum output power			-80		dBm	
Output amplitude variation @ gain control of 50%	Part – part Vdd Temperature		±4.5 ±0.5 ±3		dB dB dB	
Baseband-to-RF signal path						
Gain flatness	Over output frequency range at 90% of gain control		±1		dB	
Adjacent channel leakage rejection (ACLR1) @ rated power	f_C ± 5.0 MHz		-40	-37.5	dBc/ 3.84 MHz	1, 2, 4
Alternate channel leakage rejection (ACLR2) @ rated power	f_C ± 10.0 MHz		-57	-53	dBc/ 3.84 MHz	1, 2, 4
Rx band noise power @ rated output power and duplexer offset	UMTS 2100 Rx UMTS 1900 Rx UMTS 1700/AWS		-142 -142 -143		dBm/Hz	3
Carrier suppression	Within Tx band @ rated output power		-26	-21	dBc	
Carrier suppression	Within Tx band @ -33 dBm output power		-22		dBc	
Image suppression	from -33 dBm to rated output power		-35	-31	dBc	

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Notes for Table 3-12:

1. Measured at rated output power using specification compliant waveforms as per Annex A, Section A.2.1, Table A.1 of 3GPP Technical Specification – UE Radio Transmission and Reception (FDD), 3GPP/ TS25.101. Ratio of power in 3.84 MHz bandwidth at specified offset to in-band power.
2. Stated specification or -85 dBm, whichever is higher; measured with a filter that has a root-raised cosine (RRC) filter response, roll-off = 0.22 and a bandwidth equal to the 3.84 MHz chip rate.
3. The receive band specification is at rated average output power.
4. Evaluated with worst cases of HSDPA waveform.
5. UTRA/FDD UL Reference Measurement Channel (12.2 kbps) (12.2/60/15 kbps - info bit rate/DPDCH/DPCCH) (DPCCH/DPDCH <= 12/15), (HS-DPCCH/DPCCH = 19/15), with a root-raised cosine (RRC) filter response, roll-off alpha=0.22 and bandwidth equal to the chip rate.

3.7.2 UMTS low-band transmit signal path

Table 3-13 UMTS low-band Tx specifications

Parameter	Comments	Min	Typ	Max	Unit	Notes
RF output						
Output frequency range	UMTS 800 band UMTS 850 band UMTS 900 band	824 830 880		849 840 915	MHz MHz MHz	
Maximum output power (average channel power) UMTS800 band UMTS900 band		 7 7	 8 8		dBm dBm dBm	5
Minimum output power			-80		dBm	
Output amplitude variation @ gain control range = 50%	Part – part Vdd Temperature		±4.5 ±0.5 ±3		dB dB dB	
Baseband-to-RF signal path						
Gain flatness	Over output frequency range at 90% gain control range		±1		dB	
Gain temperature coefficient			±0.1		dB/deg C	
Adjacent channel leakage rejection (ACLR1)	f_C ± 5.0 MHz		-40	-37.5	dBc/ 3.84 MHz	1, 2, 4
Alternate channel leakage rejection (ACLR2)	f_C ± 10.0 MHz		-56	-53	dBc/ 3.84 MHz	1, 2, 4
Rx band noise power	UMTS 800 Rx: 869 to 894 MHz UMTS 850 Rx: 875 to 885 MHz UMTS 900 Rx 925 to 960 MHz @ rated output power		-141 -141 -141		dBm/Hz	3
Carrier suppression	Within Tx band @ rated output power		-26	-21	dBc	
Carrier suppression	Within Tx band @ -33 dBm output power		-21		dBc	
Image suppression	from -33 dBm to rated output power		-35	-31	dBc	

Note: See the table notes following Table 3-12 in Section 3.7.1

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3.7.3 RMS power detector

Table 3-14 RMS power detector specifications

Specification	Comments	Min	Nom	Max	Units	Note
Input frequency range	UMTS 800	824		849	MHz	
	UMTS 850	830		840	MHz	
	UMTS 1900	1850		1910	MHz	
	UMTS 2100	1920		1980	MHz	
	UMTS1700	1710		1785	MHz	
	UMTS 900	880		915	MHz	
Input RF power	50-ohm input impedance	-11	0	2	dBm	1
Output accuracy	Input RF power from -4 to 0 dBm		0.25		dB	
	Other RF powers		0.5		dB	

Note:
The output of the power amplifier is coupled to the power detector with a coupling ratio of 26 dB.

3.8 WCDMA secondary receive signal path specifications(RTR6285 only)

3.8.1 WCDMA high-band secondary receive signal path specifications

Table 3-15 WCDMA high-band DRx performance specifications

Parameter	Comments	Min	Typ	Max	Unit	Notes
RF input						
Input frequency range						
UMTS 2100		2110		2170	MHz	
UMTS 1900		1930		1990	MHz	
UMTS1700		1844.9		1879.9	MHz	
UMTS AWS		2110		2155	MHz	
Input VSWR (in-band)	50-ohm external match			2:1		
RF-to-baseband signal path						
Noise figure	Double sideband					1
Highest gain mode (G0)			3.8		dB	
Mid-high gain mode (G1)			11.5		dB	
Mid gain mode (G2)				27	dB	
Mid-low gain mode (G3)				40	dB	
Lowest gain mode (G4)				52	dB	
Output load capacitance	I and Q, each differential			8	pF	2

Notes:
1. NF = CNRin/CNRout. Double-sideband noise integrated from 1 kHz to 1.92 MHz (I).
2. Differential capacitance not to exceed 8 pF on I or Q lines to MSM. I and Q load capacitance should be equal.

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3.8.2 WCDMA low-band DRx performance specifications

Table 3-16 WCDMA low-band DRx performance specifications

Parameter	Comments	Min	Typ	Max	Unit	Notes
RF input						
Input frequency range UMTS 800 UMTS 900		 869 925		 894 960	 MHz MHz	
Input VSWR (in-band)	50-ohm external match			2:1		
RF-to-baseband signal path						
Noise figure Highest gain mode (G0) Mid-high gain mode (G1) Mid gain mode (G2) Mid-low gain mode (G3) Lowest gain mode (G4)	Double sideband		 3.5 10.5	 4.5 11.5 27 40 52	 dB dB dB dB dB	1
Output load capacitance	I and Q, each differential			8	pF	2

Notes:
1. NF = CNR_{in}/CNR_{out}. Double-sideband noise integrated from 1 kHz to 1.92 MHz (I).
2. Differential capacitance not to exceed 8 pF on I or Q lines to MSM. I and Q load capacitance should be equal

3.9 GPS path specifications(RTR6285 only)

3.9.1 GPS signal path specifications

Table 3-17 GPS signal path specifications

Parameter	Comments	Min	Nom	Max	Unit
Input frequency	L1 = 1575.42MHz	1574.40		1576.44	MHz
Input VSWR (in-band)	50-ohm external match			2:1	
Output load capacitance	I and Q, each differential			8	pF
High linearity mode					
Voltage conversion gain		79	83	85	
Noise figure			2.1	2.6	dB
Input IP3 (jammers: -17 dBm @ L1 + 138.0 MHz and -59 dBm @ L1 + 275.8 MHz)		1.4	6		dBm
Input IP2 (jammers: -20 dBm @ L1 + 135.0 MHz and L1 + 135.2 MHz)		79			dBm
Low power mode					
Voltage conversion gain		77	82	84	dB

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Table 3-17 GPS signal path specifications (continued)

Parameter	Comments	Min	Nom	Max	Unit
Noise figure			2.2	2.9	dB
Input IP3 (jammers: -38 dBm @ L1 + 138.0 MHz and -59 dBm @ L1 + 275.8 MHz)		-5	1		dBm
Input IP2 (jammers: -41 dBm @ L1 + 135.0 MHz and L1 + 135.2 MHz)		60			dBm

3.10 Transceiver LO generation specifications

The RTR6285/6280 IC includes three integrated PLL circuits:

- PLL1 supports the transceiver LO generation functions used for all GSM/EDGE (GSM 850, GSM 900, GSM 1800, and GSM 1900), transmitter for UMTS (UMTS 800, UMTS 850, UMTS 900, UMTS 1700, UMTS 1900, and UMTS 2100).
- PLL2 supports only UMTS primary and secondary Rx operation (UMTS 800/850, UMTS900, UMTS 1700, UMTS 1900, and UMTS 2100).
- PLL3 supports the GPS receive chain.

Table 3-18 RTR6285/6280 PLLs reference input specification

Specification	Comments	Min	Typ	Max	Unit
Nominal input frequency	From VCTCXO		19.2		MHz
Input impedance	2 pF parallel capacitance, typical		50		kohms
Input amplitude	AC coupled	0.8		1.0	Vpp

Table 3-19 GSM/EDGE Rx LO performance specifications

Specification	Comments	Min	Typ	Max	Units
GSM 900 (EGSM) Rx	All integer multiples of 200 kHz	925		960	MHz
GSM 850 (GCELL) Rx	All integer multiples of 200 kHz	869		894	MHz
GSM 1800 (DCS) Rx	All integer multiples of 200 kHz	1805		1880	MHz
GSM 1900 (GPCS) Rx	All integer multiples of 200 kHz	1930		1990	dBc
PLL setting time	Within ±0.1 ppm, includes coarse tuning. Measured from end of SBI to final frequency.			160	µs

Table 3-20 GSM/EDGE Tx LO performance specifications

Specification	Comments	Min	Typ	Max	Units
GSM 900 (EGSM) Tx	All integer multiples of 200 kHz	880		915	MHz
GSM 850 (GCELL) Tx	All integer multiples of 200 kHz	824		849	MHz

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Table 3-20 GSM/EDGE Tx LO performance specifications (continued)

Specification	Comments	Min	Typ	Max	Units
GSM 1800 (DCS) Tx	All integer multiples of 200 kHz	1710		1785	MHz
GSM 1900 (GPCS) Tx	All integer multiples of 200 kHz	1850		1910	dBc
PLL setting time	Within ±0.1 ppm, includes coarse tuning. Measured from end of SSBI to final frequency.			200	µs

Table 3-21 WCDMA Rx LO performance specifications

Specification	Comments	Min	Typ	Max	Units
Cell band LO frequencies	All integer multiples of 100 kHz	871.4		891.6	MHz
UMTS 900 band LO frequencies	All integer multiples of 200 kHz	927.4		957.6	MHz
IMT band LO frequencies	All integer multiples of 200 kHz	2112.4		2167.6	MHz
AWS band LO frequencies	All integer multiples of 100 kHz	2112.4		2167.6	MHz
UMTS1800 band LO frequencies	All integer multiples of 200 kHz	1807.4		1877.6	
PCS band LO frequencies	All integer multiples of 100 kHz	1932.4		1987.6	MHz
Lock time	Time to settle to 0.1 ppm frequency error. Measured from end of SBI write.		280		µs

Table 3-22 WCDMA Tx LO performance specifications

Specification	Comments	Min	Typ	Max	Units
UMTS Cell band LO frequencies	All integer multiples of 100 kHz	824		849	MHz
UMTS 900 band LO frequencies	All integer multiples of 200 kHz	880		915	MHz
UMTS 1900 band LO frequencies	All integer multiples of 100 kHz	1850		1910	MHz
UMTS 2100 band LO frequencies	All integer multiples of 200 kHz	1920		1980	MHz
UMTS AWS band LO frequencies	All integer multiples of 100 kHz	1710		1755	MHz
Lock time	Time to settle to 0.1ppm frequency error. Measured from end of SSBI write		150		µs

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4 Mechanical Specifications

The RTR6285/RTR6280 mechanical specifications are presented in this chapter, including its physical dimensions, visible markings, moisture sensitivity level, and thermal characteristics. Additional details pertaining to these topics are included in the *QFN Package User Guide* (80-V5243-1), available for download at the CDMA Tech Support website: https://support.cdmatech.com.

4.1 Device physical dimensions

The RTR6285/RTR6280 IC is available in the 68 mQFN package, which has an 8 mm x 8 mm body size with a height of 0.9 mm and a 0.4 mm pitch. The large center slug must be soldered to PCB ground for electrical ground, mechanical support, and thermal relief. For a complete detailed mechanical drawing, refer to the QUALCOMM *QFN Package User Guide* (80-V5243-1). The 68 mQFN package outline drawing is shown in Figure 4-1.

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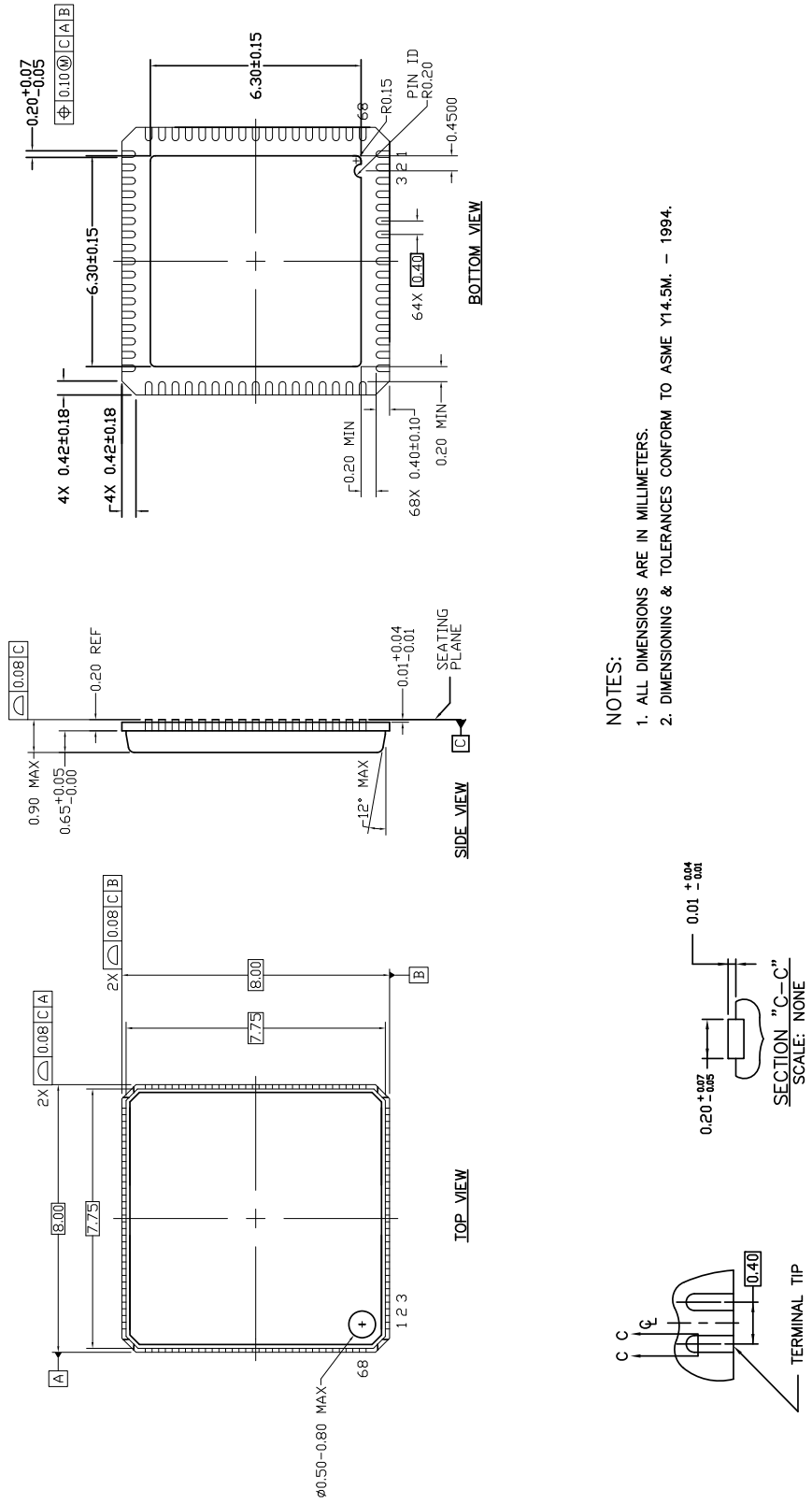


Figure 4-1 68 mQFN package outline drawing

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4.2 Part marking

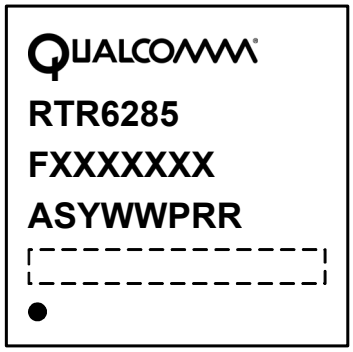


Figure 4-2 RTR6285 part marking (top view - not to scale)

Table 4-1 RTR6285 part marking line descriptions

Line	Marking	Description
1	QUALCOMM	QUALCOMM name
2	RTR6285	QUALCOMM product name ■ N = blank space: 0.18 rfcoms
3	FXXXXXXX	F = supply source code ■ F = A: TSMC, Taiwan XXXXXXX = traceability number
4	ASYWWPRR	A = assembly site code ■ A = A: Amkor, South Korea ■ A = F: ASE, South Korea S = traceability number Y = single-digit year WW = workweek (based on calendar year) P = configuration code “-P” / Configuration description: 0 / - RR = product version RR / Version description: 00 / Sample 1, HW ID = 0x00; 07 / Sample 2, HW ID = 0x08; 13 / Sample 3, HW ID = 0x10
Additional lines may appear on the part marking for some engineering samples; this is manufacturing information that is only relevant to QUALCOMM and QUALCOMM’s suppliers.		

NOTE For complete marking definitions of all RTR6285/RTR6280 IC versions, refer to the *RTR6285/RTR6280 RF Transceiver IC Revision Guide* (80-VD861-4).

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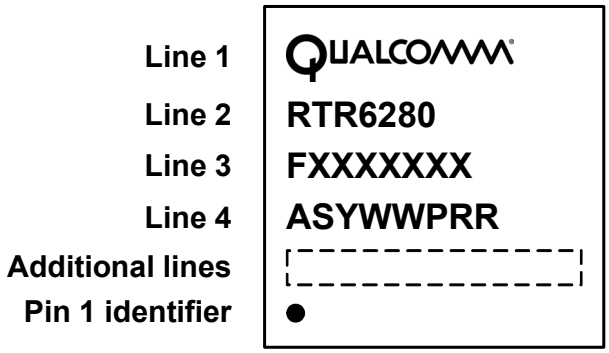


Figure 4-3 RTR6280 part marking (top view - not to scale)

Table 4-2 RTR6280 part marking line descriptions

Line	Marking	Description
1	QUALCOMM	QUALCOMM name
2	RTR6280	QUALCOMM product name ■ N = blank space: 0.18 rfcoms
3	FXXXXXXX	F = supply source code ■ F = A: TSMC, Taiwan XXXXXXX = traceability number
4	ASYWWPRR	A = assembly site code ■ A = A: Amkor, South Korea ■ A = F: ASE, South Korea S = traceability number Y = single-digit year WW = workweek (based on calendar year) P = configuration code “-P” / Configuration description: 0 / - RR = product version RR / Version description: 00 / Sample 1 HW ID = 0x08; 01 / Sample 2 HW ID = 0x10
Additional lines may appear on the part marking for some engineering samples; this is manufacturing information that is only relevant to QUALCOMM and QUALCOMM’s suppliers.		

NOTE For complete marking definitions of all RTR6285/RTR6280 IC versions, refer to the *RTR6285/RTR6280 RF Transceiver IC Revision Guide* (80-VD861-4).

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4.3 Device ordering information

To order this device, customers should provide an identification code with 19 characters as shown in Figure 4.4.

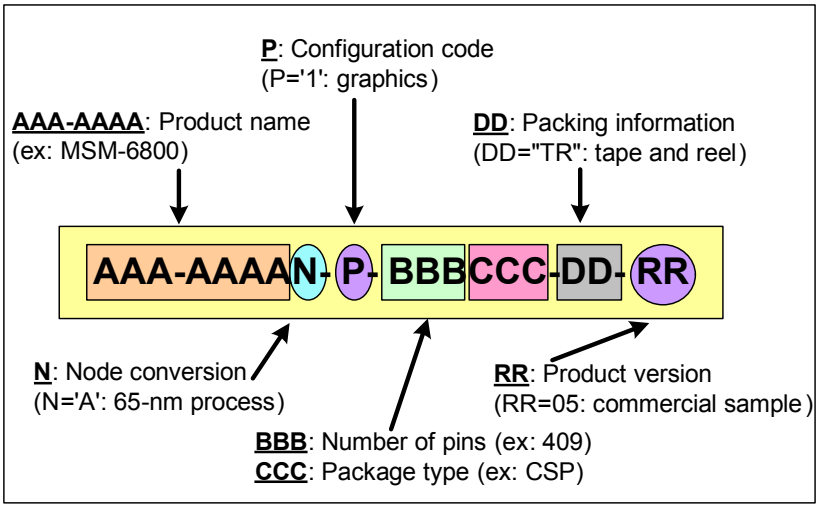


Figure 4-4 Device identification code

An example for the RTR6285 device can be as follows: RTR-6285-0-68mQFN-TR-13

To decode the information in each field, refer to Section 4.2.

4.4 Device moisture sensitivity level (MSL)

Plastic-encapsulated surface mount packages are susceptible to damage induced by absorbed moisture and high temperature. QUALCOMM follows the latest revision of the IPC/JEDEC J-STD-020 standard for moisture-sensitivity qualification. ***The RTR6285/RTR6280 IC is classified as MSL3.***

See the following sections (and their subsections) for additional MSL-related information:

- Section 5.5 – Storage conditions, unpacking, and handling
- Section 6.3 – Packing for shipment

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4.5 Device thermal characteristics

The RTR6285/RTR6280 device in its 68 mQFN package has a typical thermal resistance, as shown in Table 4-3.

Table 4-3 Device thermal resistance

Parameter		Comments	Typ	Units
θ_{JA}	Thermal resistance, J-to-A	Junction to ambient (still air)	22.1	°C/W
θ_{JC}	Thermal resistance, J-to-C	Junction to case	6.7	°C/W

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5 PCB Mounting Guidelines

Guidelines for mounting theRTR6285/RTR6280 IC onto a printed circuit board (PCB) are presented in this chapter, including land pad and stencil design details, surface mount technology (SMT) process characterization, SMT process verification, and storage recommendations after the devices are removed from their shipping packages. Additional details are available in the *QFN Package User Guide* (80-V5243-1), which can be downloaded from https://support.cdmatech.com (the CDMA Tech Support website).

The RTR6285/RTR6280 IC is lead-free internally and externally, and is RoHS-compliant. It has Sn terminal plating.

NOTE QUALCOMM defines its lead-free (or Pb-free) semiconductor products as having a maximum lead concentration of 1000 ppm (0.1% by weight) in raw (homogeneous) materials and end products. See the *IC Package Environmental Roadmap* (80-V6921-1) for discussion of the QUALCOMM package environmental programs, RoHS compliance details, and tables defining pertinent characteristics of all QUALCOMM IC products.

5.1 Land pad and stencil design

5.1.1 68 mQFN land pad and stencil design

In general, the PCB land pattern is the same size as the package terminal. Solder paste is typically printed with the same dimensions as the land pattern. *However, this is not the case for the 68 mQFN package.* Figure 5-1 shows the recommended land pattern dimensions and solder stencil dimensions.

It is recommended to use a 127 µm thick stencil. This pattern dimension is provided as a basis for SMT development using 68 mQFN packages; however, the pattern might require slight modifications to allow for equipment and material differences from those listed in this specification. It is important to fully characterize your SMT process for optimal results. Daisy chain packages are suitable for SMT characterization.

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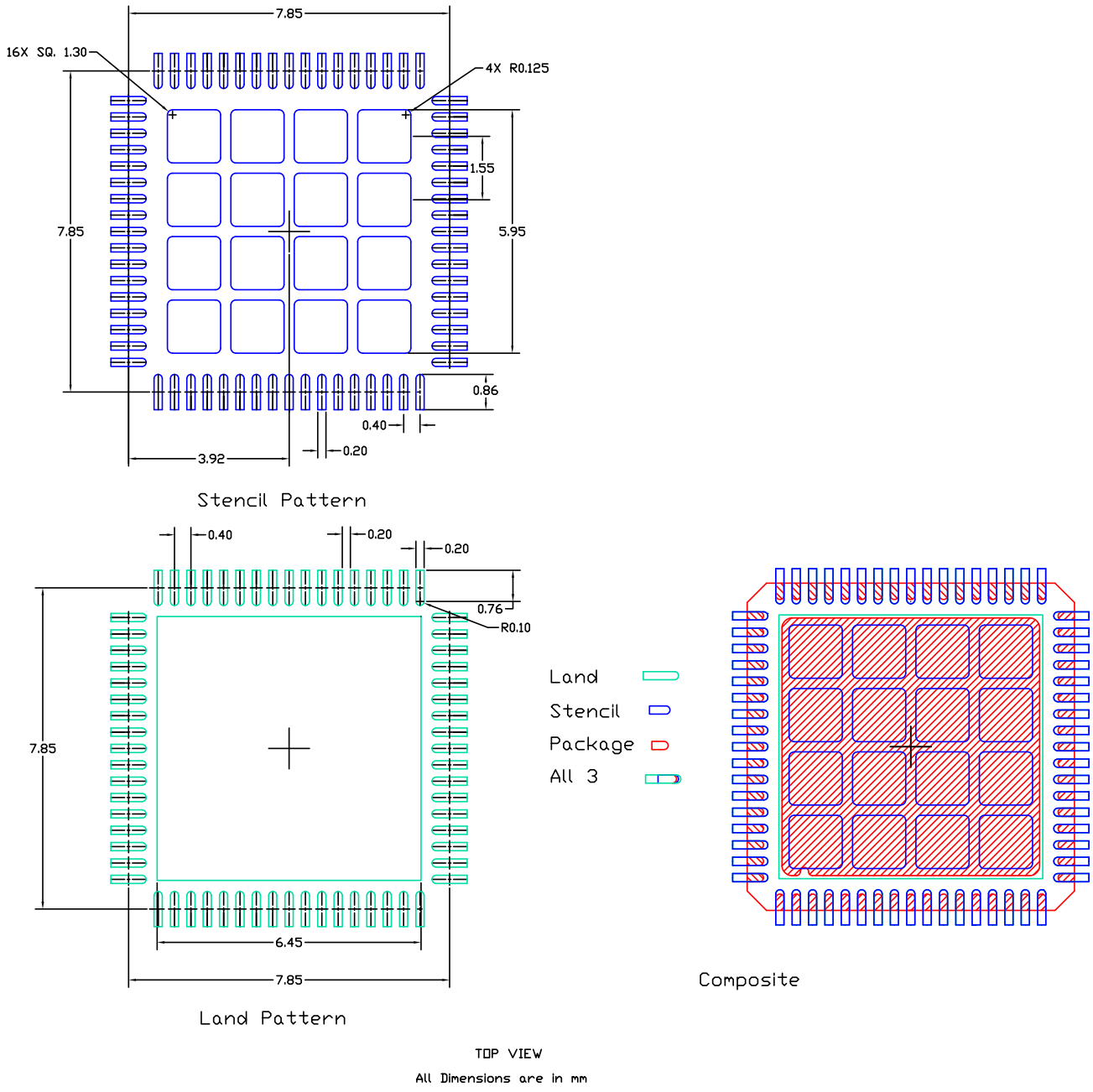


Figure 5-1 68 mQFN land and stencil pattern drawing

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5.2 SMT development and characterization

The information presented in this section describes QUALCOMM board-level characterization process parameters. It is included to assist customers when starting their SMT process development; it is not intended to be a specification for customer SMT processes.

NOTE QUALCOMM recommends that customers follow their solder paste vendor recommendations for the screen-printing process parameters and reflow profile conditions.

QUALCOMM characterization tests attempt to optimize the SMT process for the best board-level reliability possible. This is done by performing physical tests on evaluation boards, including:

- Peel test
- Bend-to-failure
- Bend cycle
- Tensile pull
- Drop shock
- Temperature cycling

QUALCOMM recommends characterizing the land patterns according to each customer's processes, materials, equipment, stencil design, and reflow profile ***prior to PCB production***. Review the land pattern and stencil pattern design recommendations in Section 5.1 as a guide for characterization.

Optimizing the solder stencil pattern design and print process is critical to ensure print uniformity, decrease voiding, and increase board-level reliability.

Daisy-chain packages are suitable and available for SMT characterization; ordering information is included in the *QFN Package User Guide* (80-V5243-1).

Reflow profile conditions typically used by QUALCOMM for SnPb and lead-free systems are given in Table 5-1.

Table 5-1 QUALCOMM typical SMT reflow profile conditions (for reference only)

Profile stage	Description	SnPb (standard) condition limits	Lead-free (high-temp) condition limits
Preheat	Initial ramp	3°C/sec max	3°C/sec max
Soak	Dry out and flux activation	135 to 165°C 60 to 120 sec	135 to 175°C 60 to 120 sec
Reflow	Time above solder paste melting point	30 to 90 sec	40 to 90 sec
	SMT peak package body temperature	230°C	245°C
Cool down	Cool rate – ramp to ambient	6°C/sec max	6 °C/sec max

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5.3 SMT peak package body temperature

QUALCOMM recommends the following limits during the SMT board-level solder attach process:

- SMT peak package body temperature of 250°C – the temperature that should not be exceeded as measured on the package body's top surface
- Maximum duration of 40 seconds at this temperature

Although the solder paste manufacturers' recommendations for optimum temperature and duration for solder reflow should be followed, the QUALCOMM-recommended limits must not be exceeded.

5.4 SMT process verification

QUALCOMM recommends verification of the SMT process prior to high-volume PCB fabrication, including:

- Electrical continuity
- X-ray inspection of the package installation for proper alignment, solder voids, solder balls, and solder bridging
- Visual inspection
- Cross-section inspection of solder joints to confirm registration, fillet shape, and print volume (insufficient, acceptable, or excessive)

5.5 Storage conditions, unpacking, and handling

Some high-level instructions for storing, unpacking, and handling RTR6285/RTR6280 devices are presented below.

5.5.1 Storage conditions

The RTR6285/RTR6280 devices, as delivered in tape and reel carriers, must be stored in sealed, moisture barrier, anti-static bags. The QUALCOMM-calculated shelf life in a sealed moisture bag is 60 months; this value requires an ambient temperature less than 40°C and relative humidity less than 90%.

5.5.2 Out-of-bag duration

The RTR6285/RTR6280 IC is classified as MSL3, and must be soldered to a PCB within its factory floor life of 168 hours (one week) after opening the moisture barrier bag (MBB).

NOTE The factory must provide an ambient temperature less than 30°C and relative humidity less than 60%, as specified in the IPC/JEDEC J-STD-033 standard.

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5.5.3 Baking

It is **not necessary** to bake the RTR6285/RTR6280 devices if the conditions specified in Section 5.5.1 and Section 5.5.2 have **not been exceeded**.

It is **necessary** to bake the RTR6285/RTR6280 devices if any condition specified in Section 5.5.1 or Section 5.5.2 has **been exceeded**. The baking conditions are specified on the moisture-sensitive caution label attached to each bag (see Figure 6-7 for details).

CAUTION If baking is required, the devices must be transferred into trays that can be baked to at least 125°C. Devices should not be baked in tape and reel carriers at any temperature.

5.5.4 Electrostatic discharge

Electrostatic discharge (ESD) occurs naturally in laboratory and factory environments. An established high-voltage potential is always at risk of discharging to a lower potential. If this discharge path is through a semiconductor device, destructive damage may result.

ESD countermeasures and handling methods must be developed and used to control the factory environment at each manufacturing site.

QUALCOMM products must be handled according to the ESD Association standard: ANSI/ESD S20.20-1999, *Protection of Electrical and Electronic Parts, Assemblies, and Equipment*.

Refer to Chapter 7 for the RTR6285/RTR6280 device ESD ratings.

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6 Packing Methods and Materials

Details about the tape and reel carrier, how it should be packed for shipment, and the materials used for packing are discussed in this chapter. Additional details are available in the *QFN Package User Guide* (80-V5243-1), which can be downloaded from the CDMA Tech Support website: https://support.cdmatech.com.

6.1 Tape and reel information

The single-feed tape carrier for the RTR6285/RTR6280 device is illustrated in Figure 6-1; this figure also shows the proper part orientation. The tape width is 16 mm and the parts are placed on the tape with a 12 mm pitch. The reels are 330 mm (13 inches) in diameter with 177.8 mm (7-inch) hubs. Each reel can contain up to 2000 devices.

6.1.1 Package orientation in carrier tape

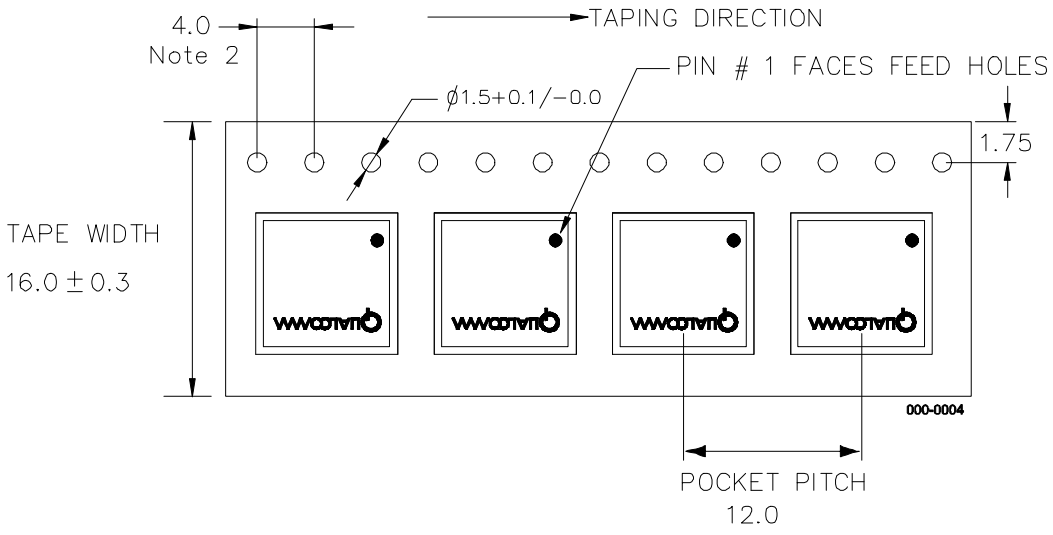


Figure 6-1 Tape dimensions for 68 mQFN

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6.1.2 Tape handling

Tape-handling recommendations are shown in Figure 6-2.

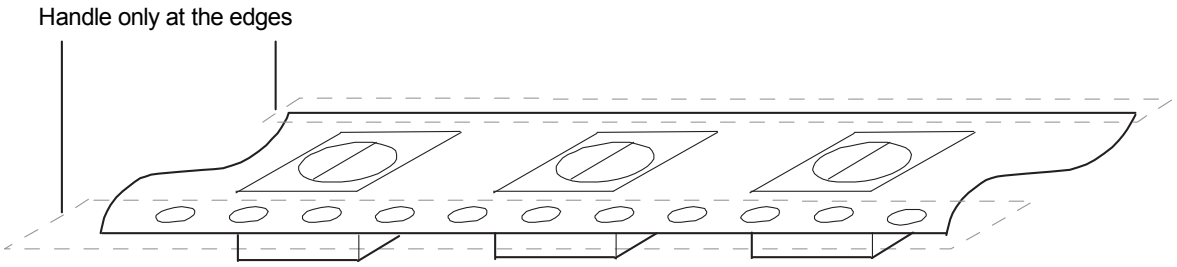


Figure 6-2 Tape handling

6.2 Barcode label

A barcode label provides necessary information for inspection and inventory control, and is attached to the reel as shown in Figure 6-3.

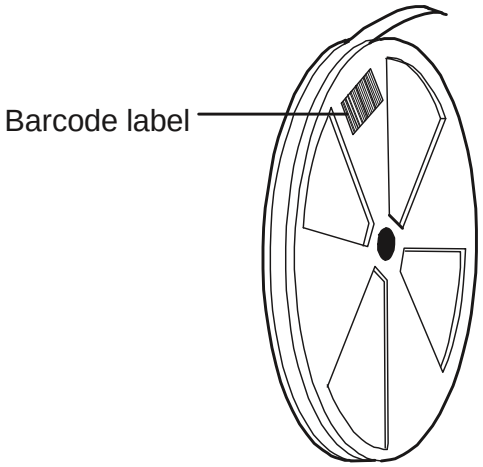


Figure 6-3 Tape and reel barcode label placement

The barcode label (Figure 6-4) includes the following items:

- Customer item ID
- QUALCOMM part number
- Lot code
- Device assembly date code

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- Description of QUALCOMM product (RTR6285/RTR6280)
  - 68 mQFN
    - RTR-6285N-P-68mQFN-TR-RR-xxxx
    - RTR-6280N-P-68mQFN-MT-RR-xxxx

  Where:

  N = node conversion

  P = configuration code

  TR = tape and reel

  MT = matrix tray

  RR = product version

  Refer to Section 4.2 for the definitions of N, P, and RR.
- SMT manufacturing process information:
  - Moisture sensitivity level (MSL3)
  - Completely lead-free Sn terminal solder composition {Pb-free (e3)}
  - Bag seal date
  - SMT peak package body temperature during SMT soldering (250°C)
- Countries of die fabrication and device assembly
- Intermediate container quantity

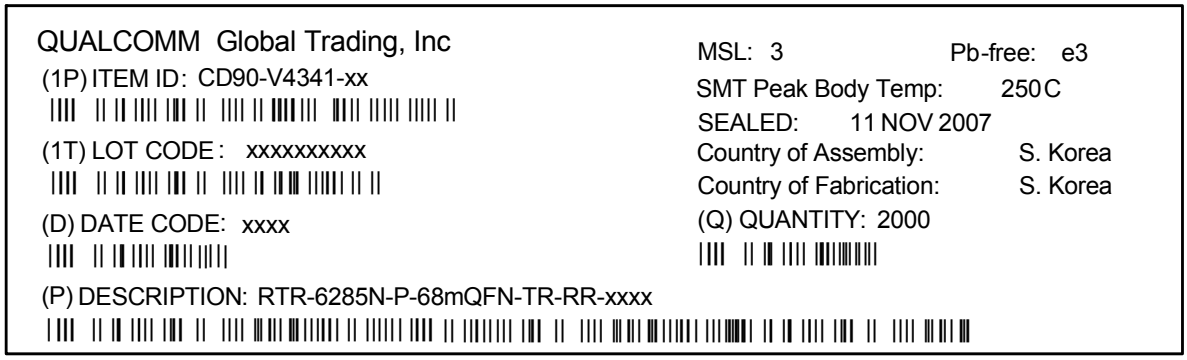


Figure 6-4 Example barcode label

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6.3 Packing for shipment

Devices can be shipped in either tape and reel carriers or trays. Tape and reel carriers used for shipping RTR6285/RTR6280 devices conform to the industry standard EIA-481 and are packed as described in this section, including the following ***required*** packing materials:

- Moisture barrier bag
- Desiccant pouches
- Humidity indicator card

Each shipment contains devices that have been baked dry and enclosed in vacuum-sealed moisture barrier bags with desiccant pouches and humidity indicator cards.

6.3.1 Moisture barrier bag with caution label

The reel (or tray) of parts is placed inside a moisture barrier bag (MBB), along with the humidity indicator card and desiccant pouches (Figure 6-5). The bag is strong, ESD-safe, and allows minimal moisture transmission. It is vacuum-sealed at the factory and should be handled carefully to avoid puncturing or tearing. This bag protects the enclosed devices from moisture exposure; it should not be opened until the devices are ready to be board-mounted. The MBB is required for RTR6285/RTR6280 devices.

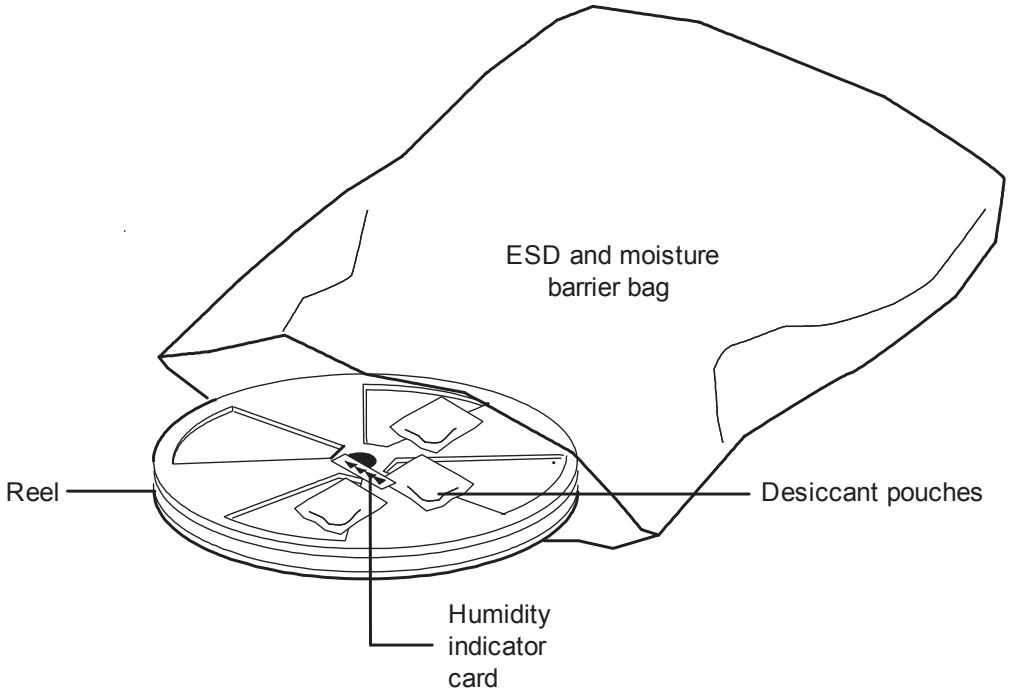


Figure 6-5 Bag packing for tape and reel

The moisture barrier bag (Figure 6-6) includes a barcode label that is identical to the label discussed in Section 6.2, and also includes moisture-sensitive caution information. This

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caution information can be printed directly onto the MBB, or it can be attached as a separate label.

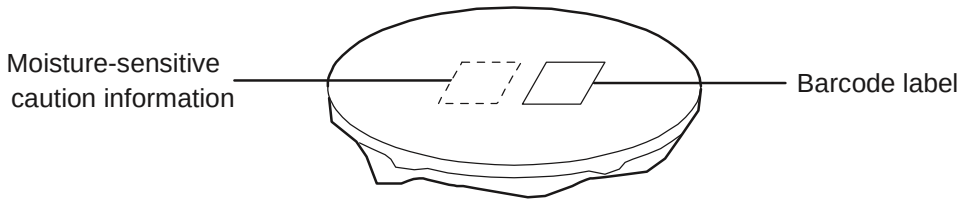


Figure 6-6 Moisture-sensitive caution information on MBB

The caution information (Figure 6-7) outlines precautions that must be taken with desiccant-packed units, including the shelf life and baking requirements. For detailed information on product shelf life, refer to *Shelf Life Definition, Calculation, and Labeling - Application Note* (80-VB459-5).



Figure 6-7 Example moisture-sensitive caution label

NOTE This moisture-sensitive caution label is in effect as of February 2007.

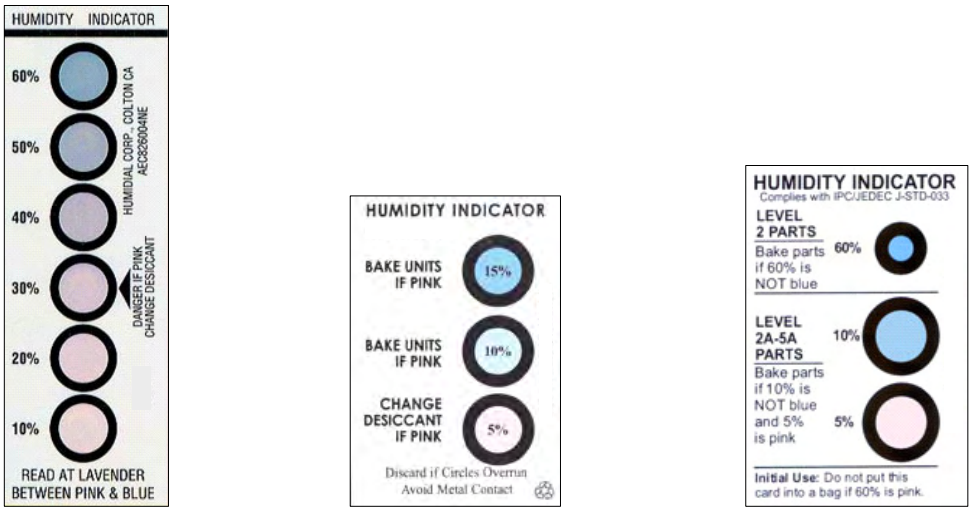
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6.3.2 Desiccant

Each MBB contains one or more desiccant pouches to absorb moisture that may be present in the bag. The humidity indicator card (Section 6.3.3) should be used as the primary method to determine whether the enclosed parts have absorbed excessive moisture. Do not bake or reuse the desiccant once it is removed from the MBB. Desiccant pouches are required for RTR6285/RTR6280 devices.

6.3.3 Humidity indicator card

Along with the desiccant pouches, the MBB contains a humidity indicator card (HIC). This card is a moisture indicator and is included to show the approximate relative humidity level within the bag. Representations of example HICs are shown in Figure 6-8. If the components have been exposed to moisture beyond the recommended limits for use in an SMT process, the units must be rebaked.



Six-button HIC Three-button 5-10-15 HIC Three-button 5-10-60 HIC

Figure 6-8 Example humidity indicator cards

A three-button 5-10-60 HIC (right side of Figure 6-8) replaces the three-button 5-10-15 HIC (middle of Figure 6-8) in some packaging to comply with new J-STD-033B specifications. The new 60% RH button on the HIC allows for identification of RH limits on MSL2 product packaging. The cards should be read as follows:

- Six-button HIC (left side of Figure 6-8):
  - For all levels of parts: If the 20% button is ***pink*** and the 30% button is ***not blue***, the components have exceeded the limit for moisture exposure and must be rebaked.

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- Three-button 5-10-15 HIC (middle of Figure 6-8):
  - For all levels of parts: If the 5% button is ***pink*** and the 10% button is ***not blue***, the components have exceeded the limit for moisture exposure and must be rebaked.
- Three-button 5-10-60 HIC (right side of Figure 6-8):
  - Level 2 parts: If the 60% button is ***not blue***, the components have exceeded the limit for moisture exposure and must be rebaked.
  - Level 2A – 5A parts: If the 10% button is ***not blue*** and the 5% button is ***pink***, the components have exceeded the limit for moisture exposure and must be rebaked.

The HIC is required for RTR6285/RTR6280 devices.

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6.4 Intermediate box

The sealed MBB is placed inside an intermediate box (Figure 6-9).

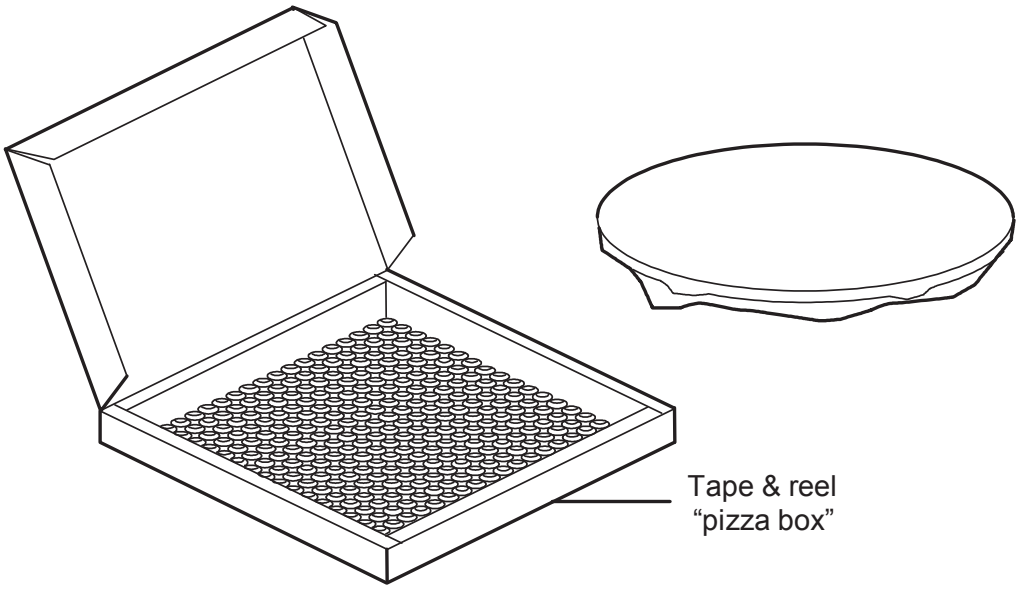


Figure 6-9 Box packing for tape and reel

A customer barcode label is placed on the intermediate box (Figure 6-10). This box may also include an optional QUALCOMM supplier label (identical to the barcode label shown in Figure 6-4).

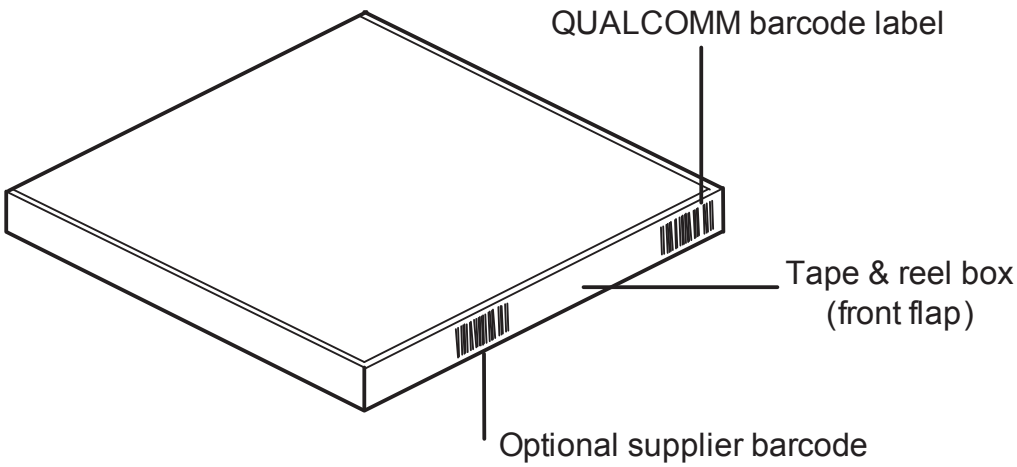


Figure 6-10 Intermediate box label placement

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7 Part Reliability Test Specification

7.1 Reliability qualification summary

Table 7-1 RTR6285 qualification summary

Tests, standards, and conditions	Sample size	Result
Early life failure rate (ELFR) HTOL JESD22-A108-A Tj 137°C, 44 hours, stress voltage = 2.25 V	1400	Pass 716 dppm @ 60% C.L.
Average failure rate (AFR) HTOL JESD22-A108-A Tj 137°C, 168 hours, stress voltage = 2.25 V	1400	Pass 20 FIT @ 60% C.L.
ESD – human body model (HBM) JESD22-A114-B	3	Pass 1500 V
ESD - charge device model (CDM) JESD22-C101-C All pins pass 500 V CDM except: VDD_DA (pin 54) passes at 200 V VDD_LNA_GPS_DX (pin 37) passes at 200 V	3	Pass 500 V
Latch-up JESD78, class II, max. temperature: 85°C I-current test: all pins pass ±100 mA except: SBDT (pin 20) passes up to -55 mA V-supply over-voltage test: all pins pass 1.4 x VDD	6	Pass
Temperature cycle JESD22-A104-B, JESD22-A113-B Temperature -55°C to +125°C, 1000 cycles **Preconditioning** JESD22-A113-B MSL 3 reflow @ 260 +0/-5°C	231 per assembly site	Pass
Highly accelerated stress test (HAST) JESD22-A110-B 130°C, 85% relative humidity, 33.3 psia, 96 hours **Preconditioning** JESD22-A113-B MSL 3 reflow @ 260 +0/-5°C	231 per assembly site	Pass

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Table 7-1 RTR6285 qualification summary (continued)

Tests, standards, and conditions	Sample size	Result
High temperature storage life JESD22-A103-B Temperature 150°C, 1000 hours	78 per assembly site	Pass
Moisture resistance test (MRT) J-STD-020A Reflow @ 260 +0/-5°C, GZFI4 passes MSL 3	78 per assembly site	Pass
Physical dimensions JESD22-B100-A	15	Pass
Internal visual 80-V0691-1	45	Pass
Solderability JESD22-B102	15	Pass
Wire ball shear JESD22-B116	15	Pass
Die shear Mil-Std-883, method 2019	15	Pass
External visual JESD22-B101	450	Pass

Qualification sample description

Device name: RTR6285

Wafer fabrication technology: 0.18 RFCMOS

Fabrication sites: TSMC Fab6

Assembly sites: Amkor, ASE

Package type: 68 mQFN

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