深圳市菲诺克科技有限公司
TEL：13600411241 QQ：3581165900

NU1007: 9V/10W Full-Bridge Power Stage for High-Integration and High-Efficiency Medium-Power Wireless Power Transmitter

1 Features

- Input Voltage: 4V to 10V
- Output Power: 10W
- Integrated High-Efficiency Full-Bridge FETs
- Integrated FET Driver Optimized for Low EMI
- Integrated 2.5V LDO to Bias External Circuit and Provide Reference Voltage
- High-Accuracy, High-Speed, Lossless Current Measurement for FOD and In-Band Communication
- Input Under-Voltage Lockout
- Short-Circuit Protection
- Thermal Shutdown
- 3mm×3mm QFN Package

2 Applications

- Wireless Power Transmitter Compliant with WPC V1.2.3 Baseline Power Profile (BPP)
- General Wireless Power Transmitter for Consumer, Industrial and Medical Applications
- Motor Drivers

3 Descriptions

NU1007 is a highly integrated 9V/10W full-bridge power stage IC optimized for wireless power transmitter solutions. It works with transmitter controller SP3100 to create a high-performance wireless power transmitter compliant with WPC 1.2.3 BPP or customized for any customer-requested solutions. The device integrates all critical functions, such as high-efficiency power FETs, low-EMI FET driver, bootstrap circuit, 2.5V LDO and lossless current measurement. The proprietary current-measurement circuit provides accurate current reading used by FOD (Foreign Object Detection) power measurement and in-band communication. It eliminates the current-sense resistor and amplifier circuit, and thus saves cost and improves efficiency.

The IC also includes protection functions such as input under-voltage lockout, short-circuit protection, and thermal shutdown. These provisions further enhance the reliability of the total system solution.

The device is housed in a thermally enhanced 16-pin 3mm×3mm QFN package.

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4 Pin Configuration and Functions

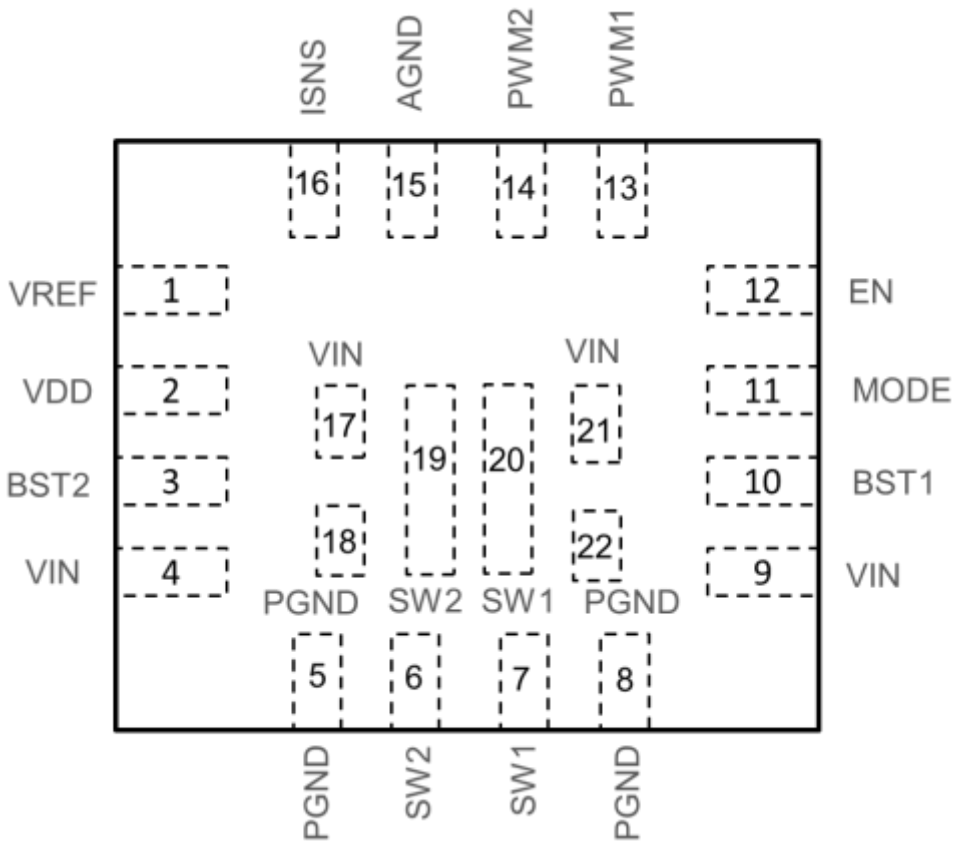


Figure 1. Top View（16-Pin QFN）

Pin		I/O	Description
Name	No.		
VREF	1	O	Output of the 2.5V LDO
VDD	2	I	Signal power input pin
BST2	3	I/O	Supply rail for the high-side gate driver of Q3 as shown in the **Block Diagram**. Connect a ceramic capacitor between the BST2 and SW2 pins
VIN	4,9, 17, 21	I	Power input pin. This pin is connected to the input of the full-bridge circuit.
PGND	5,8, 18, 22	-	Power-ground pin. This pin is connected to the ground of the full-bridge circuit.
SW2	6, 19	O	Switch node of the half-bridge FETs Q3 and Q4, as shown in the **Block Diagram**.
SW1	7, 20	O	Switch node of the half-bridge FETs Q1 and Q2, as shown in the **Block Diagram**.

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BST1	10	I/O	Supply rail for the high-side gate driver of Q1. Connect a ceramic capacitor between the BST1 and SW1 pins
MODE	11	I	Logic input to program the PWM1 and PWM2 function. See **Application Description** for details. MODE logic is detected at power-up, and can only be reset with power recycling.
EN	12	I	Enable input of the IC. Pull the pin low or keep it floating to disable the IC and open all the FETs. Logic HIGH enables the IC. The EN pin voltage needs to stay below the voltage of the VDD pin. Otherwise, a resistor of 1KΩ is recommended in series with the pin to limit its current.
PWM1	13	I	PWM logic input to the FET Q1 and Q2 as shown in the **Block Diagram**. Logic HIGH turns on the high-side FET Q1, and turns off the low-side FET Q2. Logic LOW turns on the low-side FET Q2 and turns off the high-side FET Q1. When PWM input is in the tri-state mode, both Q1 and Q2 are turned off. The switching slew rate and dead-time are internally controlled by the IC.
PWM2	14	I	PWM logic input to the FET Q3 and Q4 as shown in the **Block Diagram**. Logic high turns on the high-side FET Q3, and turns off the low-side FET Q4. Logic low turns on the low-side FET Q4 and turns off the high-side FET Q3. When PWM input is in the tri-state mode, both Q3 and Q4 are turned off. The switching slew rate and the dead time are internally controlled by the IC.
AGND	15	-	Analog ground of the IC
ISNS	16	O	Current sense output. When connected with an external resistor, the voltage at the pin is proportional to the input current.

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5 Specifications

5.1 Absolute Maximum Ratings

	MIN	MAX	UNIT
SW1, SW2 to PGND	-0.3	12	V
SW1, SW2 to PGND (<30ns)	-2	15	V
VIN to PGND	-0.3	12	V
VIN to VDD	-0.3	7	V
PWM1, PWM2, VREF, VDD, EN, MODE, ISNS to AGND	-0.3	7	V
BST1 to PGND	-0.3+SW1	7+SW1	V
BST2 to PGND	-0.3+SW2	7+SW2	V
Operating junction Temperature, T_J	-40	125	°C
Storage Temperature, T_{stg}	-55	150	°C

5.2 ESD Ratings

		UNIT
Human-Body Model	±1000	V
Charged-Device Model	±500	V

5.3 Package Thermal Ratings

		UNIT
Junction-to-ambient thermal resistance, $R_{\Theta JA}$	64.3	°C/W

5.4 Electrical Characteristics

VIN=9V, VDD=5V, Fsw=200KHz, T_j=-40 °C to 125°C(unless otherwise noted)

PARAMETERS		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT						
V_{UVLO}	Under-voltage lock out threshold	VDD ramps up	3.3	3.6	3.8	V
V_{UVLO_HYS}	Under-voltage lock out hysteresis voltage	VDD ramps down		400		mV
I_{VIN}	Input power operating current	No switching, EN=logic high			2	mA
I_{VDD}	Operating supply current	No switching, EN=logic high			0.4	mA
I_{SD_VIN}	Input shutdown current	T_j=-40°C to 85°C,			105	μA

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		EN=logic low,				
$I_{SD_VIN_4V}$	Input shutdown current at 4V input voltage	T_j=-40°C to 85°C, EN=logic low, VIN=4V			45	μA
I_{SD_VDD}	Digital shutdown current	T_j=-40°C to 85°C, EN=logic low			0.5	μA
POWER DEVICES and DRIVERS						
I_{SW_LEAK}	SW pin leakage current	Vsw=9V or Vsw=0V			1	mA
V_{BST_FW}	Bootstrap forward voltage	I_{BST}=300 μA			500	mV
I_{BST_LEAK}	Bootstrap leakage current	V_{BST}=5V, Vsw=0V			1500	nA
PWM, MODE and ENABLE INPUTS						
V_H	PWM logic high	Input rising	2.65			V
V_L	PWM logic low	Input falling			0.45	V
V_{TRI}	Tri-state voltage	Input rising and falling	1.2		1.9	V
T_{ACT}	Tri-state activation timing			100		ns
V_{EH}, V_{MODEH}	EN pin and MODE pin high	Input rising	2.65			V
V_{EL}, V_{MODEL}	EN pin and MODE pin low	Input falling			0.45	V
I_{PWM}	PWM pin input bias current	V_{PWM}=logic high		15		μA
		V_{PWM}=logic low		-15		μA
R_{EN}	Enable pin input impedance	Pull down to GND		1		MΩ
REFERENCE OUTPUT						
V_{REF}	2.5V reference voltage	Temp, line and load	2.45	2.5	2.55	V
I_{REF}	Reference-voltage maximum supply current		10			mA
PROTECTIONS						
T_{OTP}	Over-temperature protection point	Temp rising		155		°C
T_{OTP_HYS}	Over-temperature protection hysteresis	Temp rising and falling		30		°C
I_{SC}	High-side short-circuit protection point	Isc		8		A
T_{SC}	SC protection time-out period			20		ms
Current Sense						
K_{sns}	Current amplification factor, I_{vin}/ I_{sns}	I_{VIN} =1.6A Tj=0 °C to 125 °C	6624	6900	7176	
I_{offset}	Current amplification offset, I_{sns} *K_{sns} –I_{vin}	I_{VIN} =1.6A Tj=0 °C to 125 °C	-48	0	48	mA

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6 Block Diagram

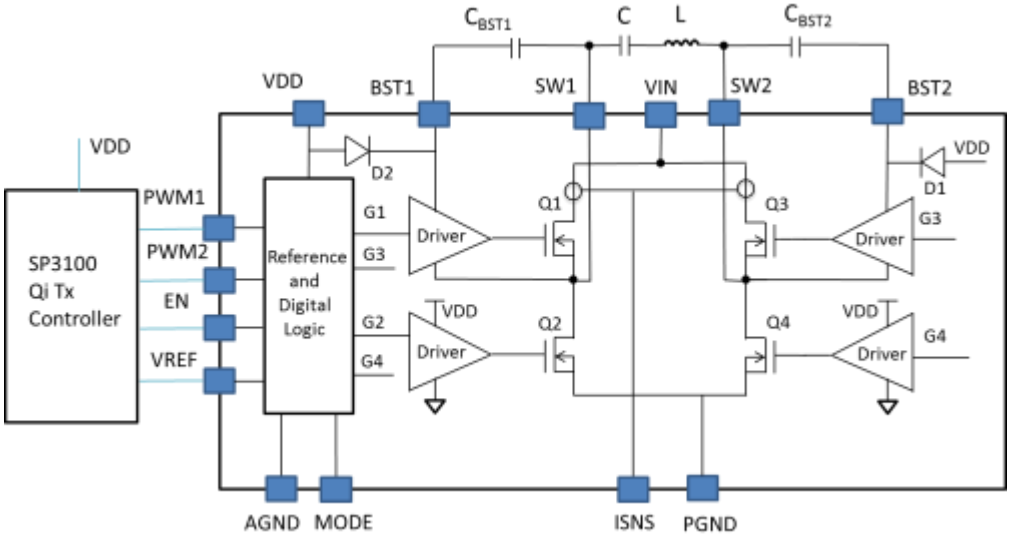


Figure 2. block diagram

7 Typical characteristics

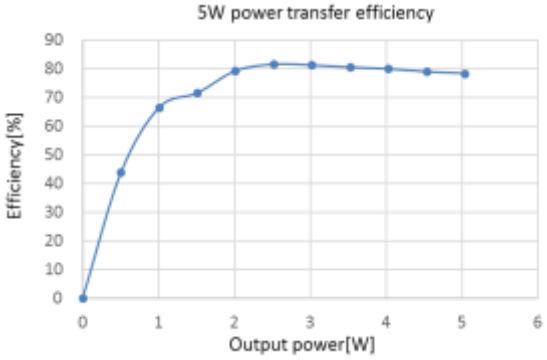


Figure 3. Efficiency vs. Power at Vout=5V

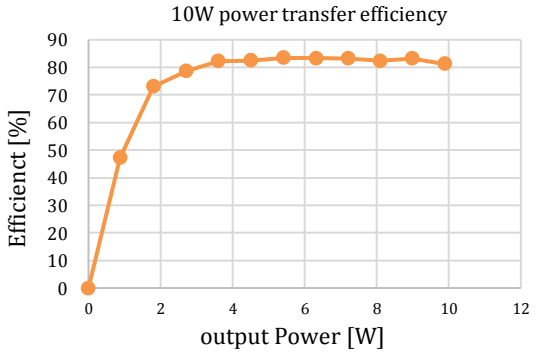


Figure 4. Efficiency vs. Power at Vout=9V

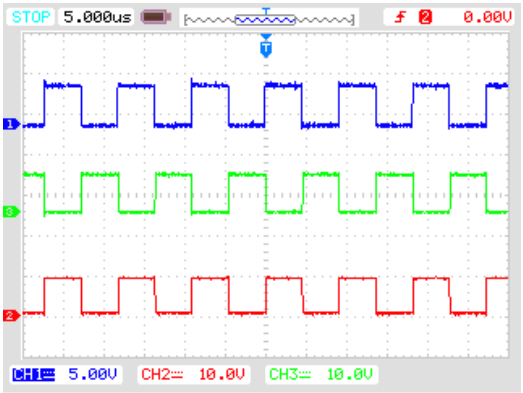


Figure 5. MODE=0, Duty=50%

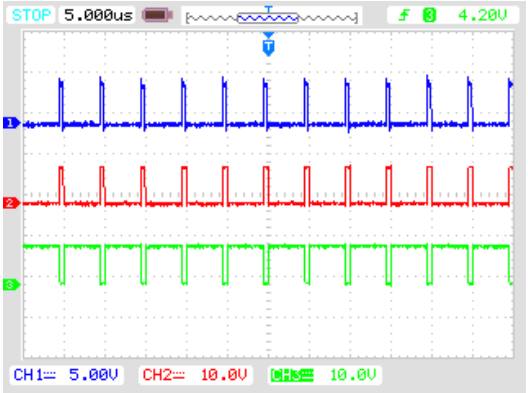


Figure 6. MODE=0, Duty=10%

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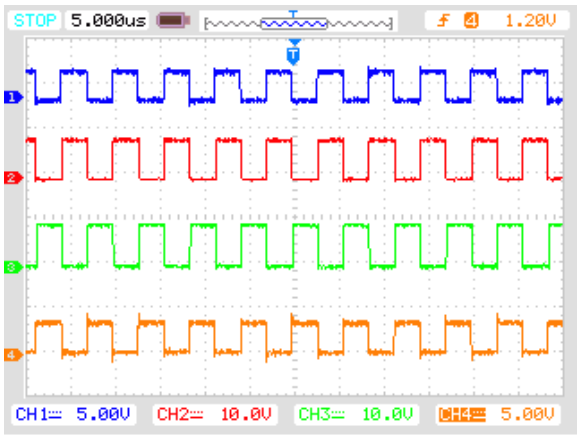


Figure 7. MODE=1, Duty=50%:

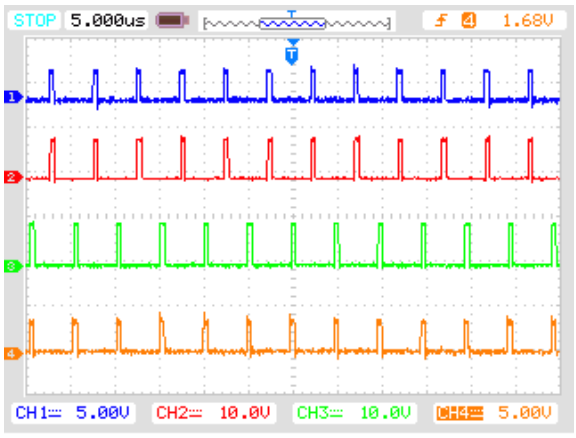


Figure 8. MODE=1, Duty=10%:

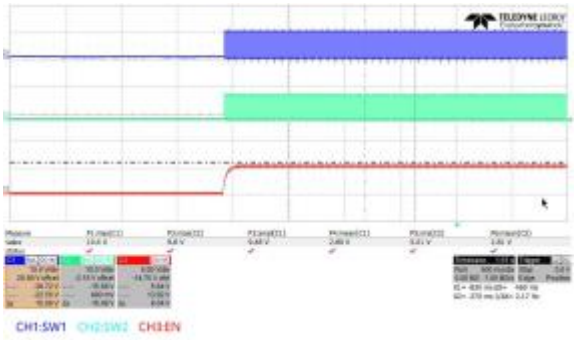


Figure 9. EN startup

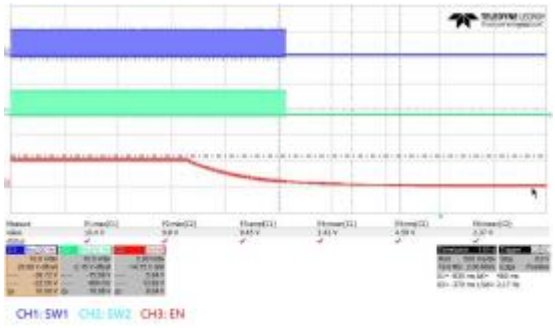


Figure 10. EN shutdown

8 Application Descriptions

8.1 Input Voltage

The IC has two power input pins. VIN is connected to the power FETs of the full bridge, and conducts high currents for power transfer. Connect a decoupling capacitor of no less than 10μF close to the pin to filter the switching current.

VDD is an analog power input pin, which is used to power IC analog signal and digital circuit including the 2.5V LDO. An Under-voltage Lockout (UVLO) circuit monitors the voltage of this pin and disables the IC operation when the VDD voltage falls below the UVLO threshold.

For normal operation, it is recommended to apply VDD voltage no larger than VIN, and no less than “VIN-7V”.

8.2 MODE and PWM Control

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When the MODE pin is at logic HIGH, the PWM1 input controls the PWM of Q1 and Q2, and the PWM2 input controls the PWM of Q3 and Q4 as shown in the **Block Diagram** (Figure. 2). The PWM1 and PWM2 can independently control the SW1 and SW2 duty cycle and frequency. For a typical WPC transmitter, the PWM1 and PWM2 are complementary in logic and have 50% duty cycle in the frequency range of 100KHz to 205KHz. When reaching 205KHz, the duty cycle of PWM1 and PWM2 can be reduced below 50% to further limit the power output.

When the MODE pin at logic LOW, the PWM2 input is disabled, and the PWM1 input controls all 4 FET switches. Logic HIGH at the PWM1 input turns on Q1 and Q4 and keeps Q2 and Q3 off. Logic LOW flips the on/off states of all 4 switches. In a typical WPC wireless power transmitter, the frequency and duty cycle of the PWM1 input are modulated to regulate the transmitter's power output.

The logic of the MODE pin is detected and latched during IC power up. In order to change the MODE logic, the IC has to go through a POR (power-on-reset) event.

When PWM input logic first enters tri-state either from logic HIGH or logic LOW, the ON or OFF states of its controlled FETs stay the same. If the PWM input stays in the tri-state for more than T_{ACT}, its controlled FETs are all turned off, and the corresponding SW output becomes high impedance. The FETs stay off until the PWM logic reaches logic HIGH or logic LOW threshold. This operation applies to both MODE logics.

8.3 Short Circuit Protection

NU1007 integrates a reliable short-circuit protection circuit. It protects the input power source and IC if the SW pin is shorted to the ground either directly or indirectly due to external component failures.

Current of the high-side FET Q1 and Q3 is sensed and compared to the short-circuit protection threshold (Isc) during every switching cycle. In each cycle, if the current exceeds the threshold, the internal up-and-down counter counts up by 1. If the current signal fails to reach the threshold during a switching cycle, the counter counts down by 1 until reaching 0. If the output of the counter reaches 7, the short circuit protection is triggered, and all 4 internal FETs are turned off regardless of the PWM inputs. The IC will attempt to restart after a time-out period of 20ms typically.

8.4 VREF Output

The VREF pin is connected to the 2.5V output of an integrated LDO. The guaranteed maximum output current of the LDO is 10mA. The accuracy of the VREF voltage is ±2.0% across temperature, line and load. Therefore, it can be used as the supply voltage as well as a reference voltage to external IC and circuit. To use with SP3100, connect the VREF pin of NU1007 to the reference input pin of the controller. It is recommended to connect a decoupling capacitor of 1μF to 10μF to the VREF pin. Capacitor values outside the range

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may cause instability of the internal linear regulator. A minimum resistor load of 5KΩ is recommended at the VREF output.

8.5 Current Sense

NU1007 has a unique current-sense circuit that measures input current and reports it on the I_{SNS} pin. The output current on the ISNS pin is directly proportional to the input current, and the ratio is defined by parameter K_{SNS} listed in the **Specifications** (Sec. 5).

Two resistors, as shown in the circuit of Figure. 11, can be connected to the pin to generate a voltage proportional to the input current. Select the resistor using the following equation(1)and(2).

The current to voltage conversion gain of ISNS is equal to the parallel resistance of Rsns1 and Rsns2.

$$Rsns = Rsns1||Rsns2 = \frac{(Vsns-Vsns_dc)*Ksns}{Iin} \qquad \text{---------(1)}$$

A pull-up resistor, as shown in the circuit of Figure. 11, can be used to create a DC bias voltage for the current signal. The DC bias voltage is given by

$$Vsns_dc = VREF * \frac{Rsns1}{Rsns1+Rsns2} \qquad \text{----------(2)}$$

A minimum resistor load of 5KΩ is recommended for the VREF output to ensure the accuracy of the ISNS output.

Where:
Rsns1 = resistor connected to the ISNS pin and AGND
Rsns2 = resistor connected to the ISNS pin and VREF pin
V_{sns} = voltage at the ISNS pin
I_{in} = input current
V_{sns} = DC bias voltage at the ISNS pin

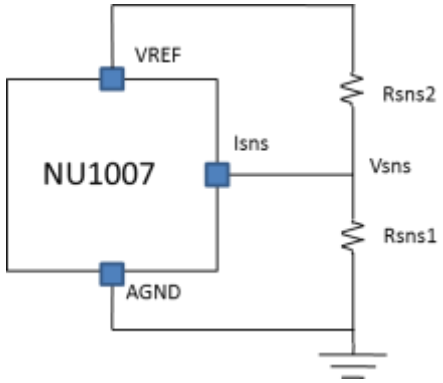


Figure 11. ISNS pin resistor connection

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8.6 Layout Guidelines

Careful PCB layout is critical to system operation. Many references are available on proper PCB layout techniques.

The NU1007 layout requires a 4-layer PCB layout for adequate ground plane. A 2-layer PCB can also be achieved at the cost of larger PCB size.

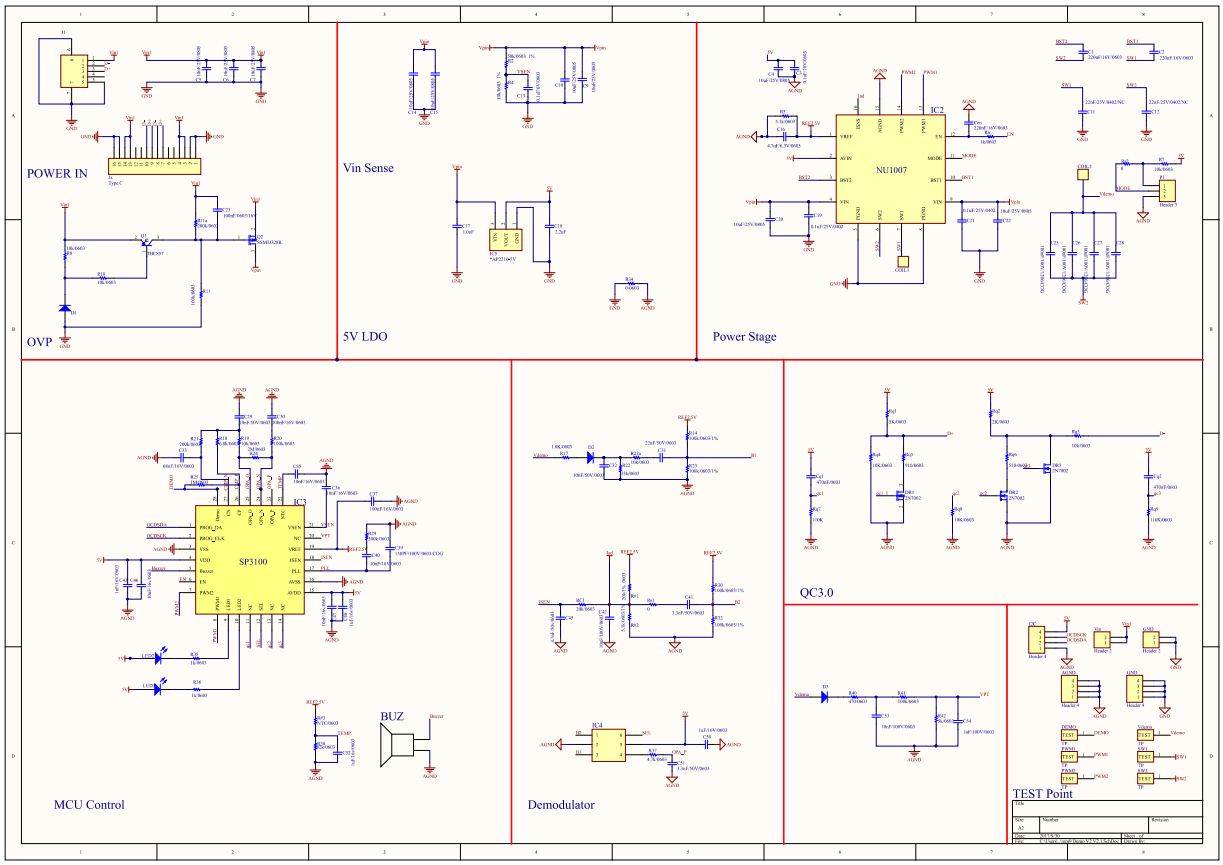
- Layer 1: Component placement, major routing and as much ground plane as possible
- Layer 2: Minor routing, a clean power-ground plane below NU1007 and power trace; a clean analog-ground plane below SP3100 and signal trace
- Layer 3: Minor routing, power trace routing, signal-trace routing and as much ground plane as possible
- Layer 4: Minor routing, a clean power-ground plane below NU1007 and power trace; a clean analog-ground plane below SP3100 and signal trace

Additionally, here are the guidelines to follow:

- Make routing loop as small as possible, especially the power loop, to minimize EMI noises.
- Place power and signal traces on Middle layer 3 to avoid noise coupling.
- Widen the copper between SW1, SW2 and LC tank, because high current in the LC tank can cause power losses on the traces and hence low efficiency. Moreover, the Vin routing should be as wide as possible.
- Separate the analog-ground plane from the power-ground plane, and use only one point to join them. Please refer to the R34 of Figure 12.
- The full-bridge power stage is integrated in NU1007, so thermal vias are needed to provide a thermal path for the NU1007.
- Place small-size input capacitors as close as possible between the Vin pin and PGND pin. These capacitors can effectively filter out high-frequency noises due to their low ESR and ESL. Please refer to C19 and C21 in Figure 12.
- Keep analog-ground plane and power-ground plane low impedance. Use as much copper as possible and an appropriate number of vias.

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9 Typical Application Circuit



10 Layout Examples

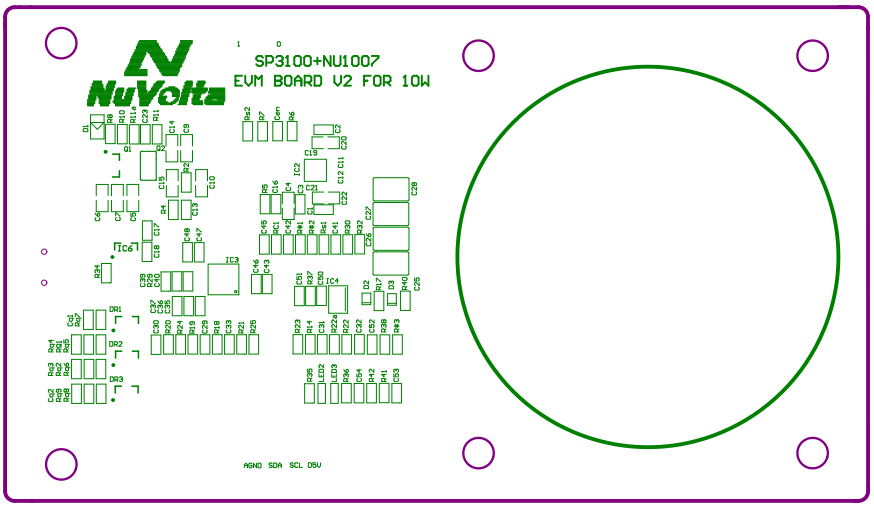


Figure 12. Top Overlay

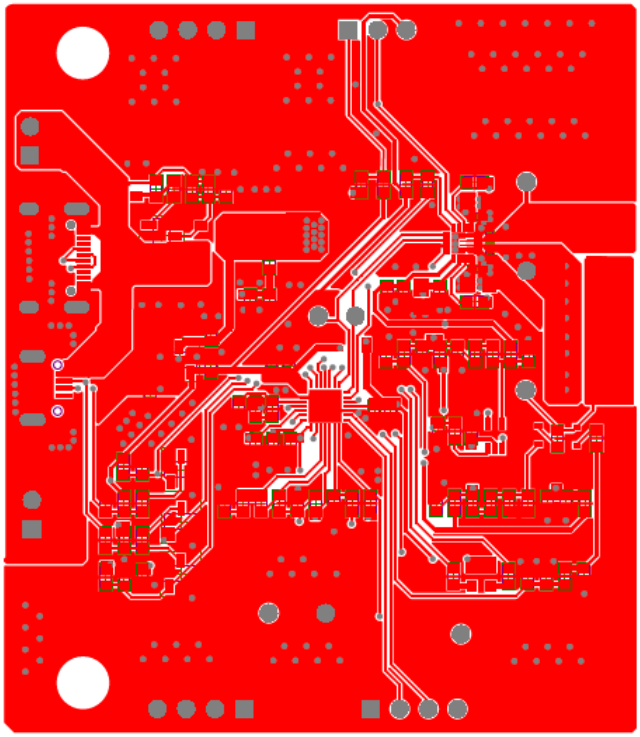


Figure 13. Top Layouts

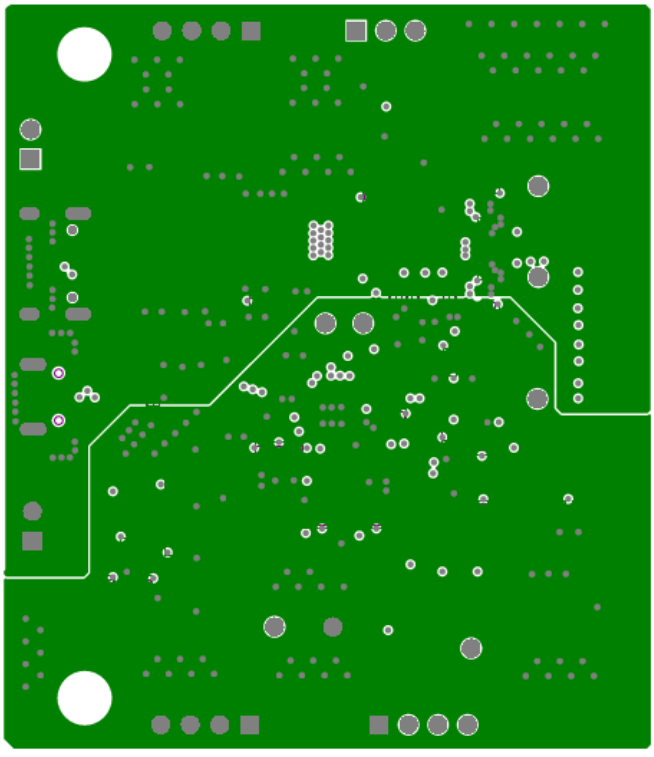


Figure 14. Middle Layer2

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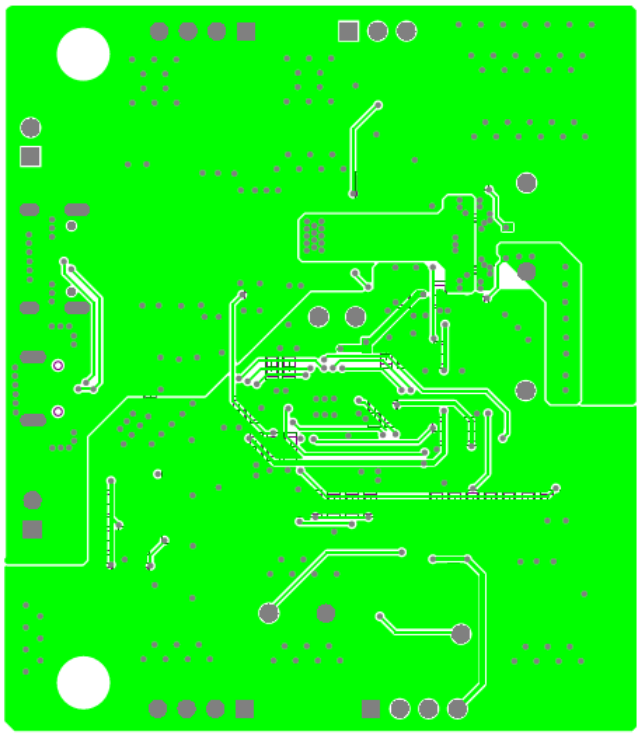


Figure 15. Middle Layer3

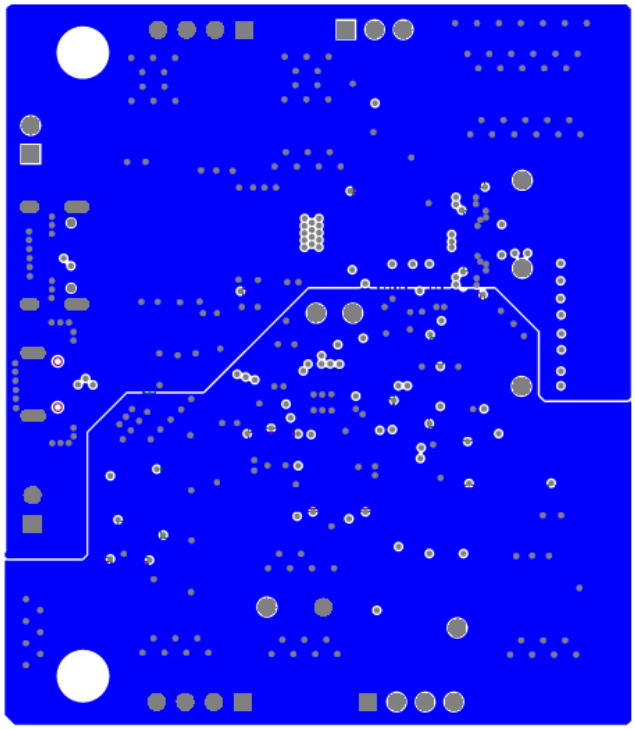


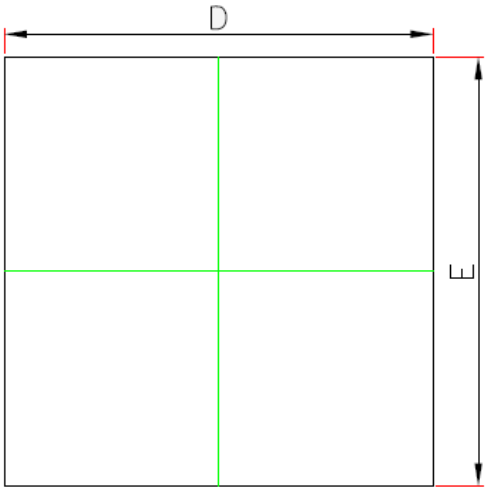
Figure 16. Bottom Layer

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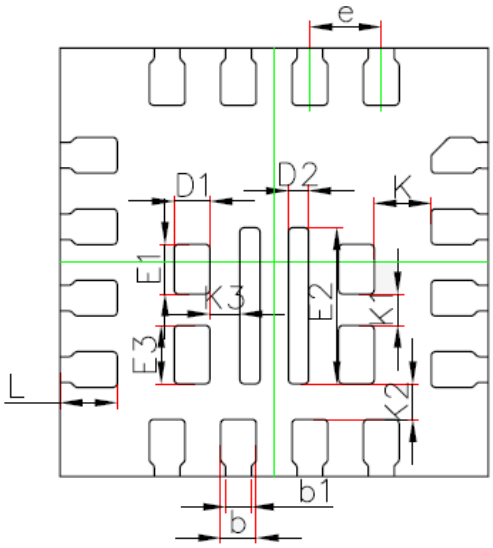
11 Package Information

Orderable Device	Status	Package Type	Package Drawing	Pins	Package Quantity	Eco Plan	Lead/Ball Finish	MSL Peak Temp	Op Temp ©	Device Marking
NU1007QDCB	Fab	QFN	QDC	16	3000	Green (RoHS & no Sb/Br)	NiPdAu	Level-2	-40 to 125	NU1007Q DC

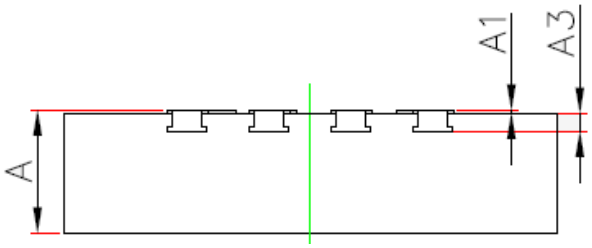
12 Mechanical Data



Top view



Bottom view



Side view

Symbol	Dimensions In Millimeters		Dimensions in Inches	
	Min	Max	Min	Max
A	0.700	0.800	0.028	0.031
A1	0.004	0.046	0.000	0.002
A3	0.110REF		0.004REF	
D	2.900	3.100	0.114	0.122
D1	0.150	0.350	0.006	0.014
E	2.900	3.100	0.114	0.122
E1	0.248	0.448	0.010	0.018
D2	0.041	0.241	0.002	0.009
E2	0.993	1.193	0.039	0.047
E3	0.309	0.509	0.012	0.020
b	0.200	0.300	0.008	0.012
b1	0.130	0.230	0.005	0.009
e	0.500TYP		0.020TYP	
L	0.300	0.500	0.012	0.020
k	0.399REF		0.016REF	
k1	0.220REF		0.009REF	
k2	0.250REF		0.010REF	
K3	0.210REF		0.008REF	

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13 Revision Histories

Revision No.	Date	Changes
V0.7	4/19/17	First draft of NU1007 datasheet
V0.8	5/17/17	Update the IC validation data
V0.81	5/26/17	Waveform of IC testing
V0.82	6/07/17	polishing and correcting English writing
V0.83	6/16/17	Update PCB layout and QC3.0 fast charge
V1.0	9/10/17	Update PCB layout

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