NTAG203F

NFC Forum Type 2 Tag compliant IC with 144 bytes user memory and field detection

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Product data sheet
COMPANY PUBLIC

1. General description

NXP Semiconductors has developed NTAG203F - NFC Forum Type 2 Tag compliant IC - to be used with NFC enabled devices according to NFC Forum technical specifications (see Ref. 8 and Ref. 9), according to NFC Forum recommendations or Proximity Coupling Devices (PCD), according to ISO/IEC 14443A (see Ref. 1). The communication layer (RF Interface) complies to parts 2 and 3 of the ISO/IEC 14443A standard. The NTAG203F is primarily designed for NFC Forum Type 2 Tag applications in electronics (i.e. connection handover, Bluetooth simple pairing, Wi-Fi Protected set-up, device authentication, gaming and others).

1.1 Contactless energy and data transfer

Communication to NTAG can be established only when the IC is connected to an antenna. Form and specification of the coil is out of scope of this document. For details on how to design antennas see Ref. 6.

When the NTAG is positioned in the RF field, the high speed RF communication interface allows the transmission of the data with a baud rate of 106 kbit/s.

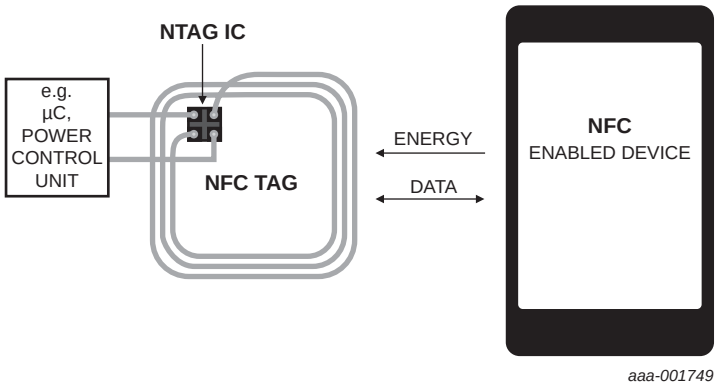


Fig 1. NFC Tag interacting with NFC enabled device

1.2 Naming conventions

Table 1. Short naming convention (for easier product identification)

Family name	Description
NTAG	NXP NFC Tag product family name
2	Platform indicator
0	Generation number (starting from 0)
3	Code number for size (0: < 64 bytes, 1: 64-96 bytes; 2: 96-128 bytes; 3: 128-256 bytes)
F	HXSON4 package with Field Detection pin

2. Features and benefits

2.1 RF Interface (ISO/IEC 14443A)

- Contactless transmission of data and supply energy (no battery needed)
- Operating distance: up to 100 mm (depending on various parameters as e.g. field strength and antenna geometry)
- Operating frequency: 13.56 MHz
- Fast data transfer: 106 kbit/s
- High data integrity: 16-bit CRC, parity, bit coding, bit counting
- True anticollision
- 7 byte serial number (cascade level 2 according to ISO/IEC 14443-3)

2.2 EEPROM

- 168 bytes of total memory, divided in 42 pages (4 bytes each)
- 144 bytes of user r/w memory area, divided in 36 pages (4 bytes each)
- Field programmable read-only locking function per page 16 pages (64 bytes) of the memory
- Field programmable read-only locking function per block (2 pages)
- 32-bit user definable One-Time Programmable (OTP) area
- 16-bit counter
- Data retention of 10 years
- Write endurance 10000 cycles

2.3 NFC Forum Tag 2 Type compliance

NTAG203F IC provides full compliance to the NFC Forum Tag 2 Type technical specification (see Ref. 8) and enables NDEF data structure configurations (see Ref. 9).

2.4 Field detection

NTAG203F features an additional RF field detection functionality. The corresponding output signal can be used as interrupt source to e.g. wake up an embedded microcontroller or trigger further actions. Typical applications are Bluetooth and Wi-Fi pairing.

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For detailed information refer to Application note Ref. 11 “AN11141 How to use the FD pin”.

2.5 Security

- Anti-cloning support by unique 7-byte serial number for each device
- 32-bit one way counter
- Field programmable read-only locking function per page for first 16 pages (64 bytes) of the memory
- Read-only locking per block for rest of memory

2.6 Cascaded UID

The anticollision function is based on an IC individual serial number called Unique IDentifier. The UID of the NTAG203F is 7 bytes long and supports cascade level 2 according to ISO/IEC 14443-3.

2.7 Anticollision

An intelligent anticollision function according to ISO/IEC 14443 allows to operate more than one tag in the field simultaneously. The anticollision algorithm selects each tag individually and ensures that the execution of a transaction with a selected tag is performed correctly without data corruption resulting from other tags in the field.

3. Ordering information

Table 2. Ordering information

Type number	Package		
	Name	Description	Version
NT2H0301F0DTL	HXSON4	plastic thermal enhanced extremely thin small outline package; no leads; 4 terminals; body 2.0 x 1,5 x 0,5 mm	-

4. Block diagram

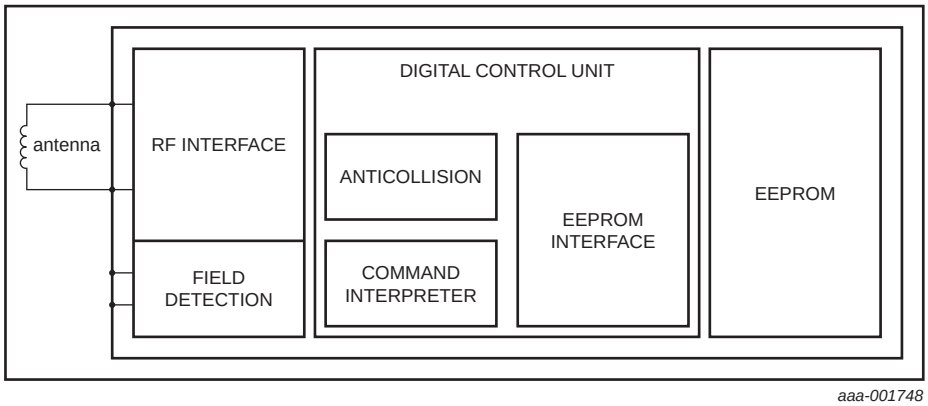
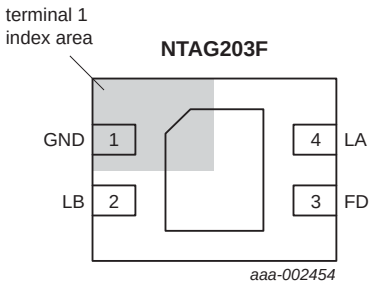


Fig 2. Block diagram

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5. Pinning information



Transparent top view

Fig 3. Pin configuration for SOT1312AB2 (HXSON4)

Table 3. Pin description of the HXSON4 package

Contactless interface module		NTAG203F
Antenna contacts	**Symbol**	**Description**
Pin 1	GND	Ground
Pin 2	LB	Antenna connection LB
Pin 3	FD	RF Field Detect connection
Pin 4	LA	Antenna connection LA

6. Marking

6.1 Marking HXSON4

Table 4. Marking HXSON4 (NTAG203F)

Type number	Description	
NT2H0301F0DTL	Marking Line A	N1F
	Marking Line B	yww

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7. Functional description

7.1 Block description

The NTAG203F chip consists of the 168 bytes of the total EEPROM memory organized in 42 pages each 4 bytes. 144 bytes (36 pages) are available for the user defined data.

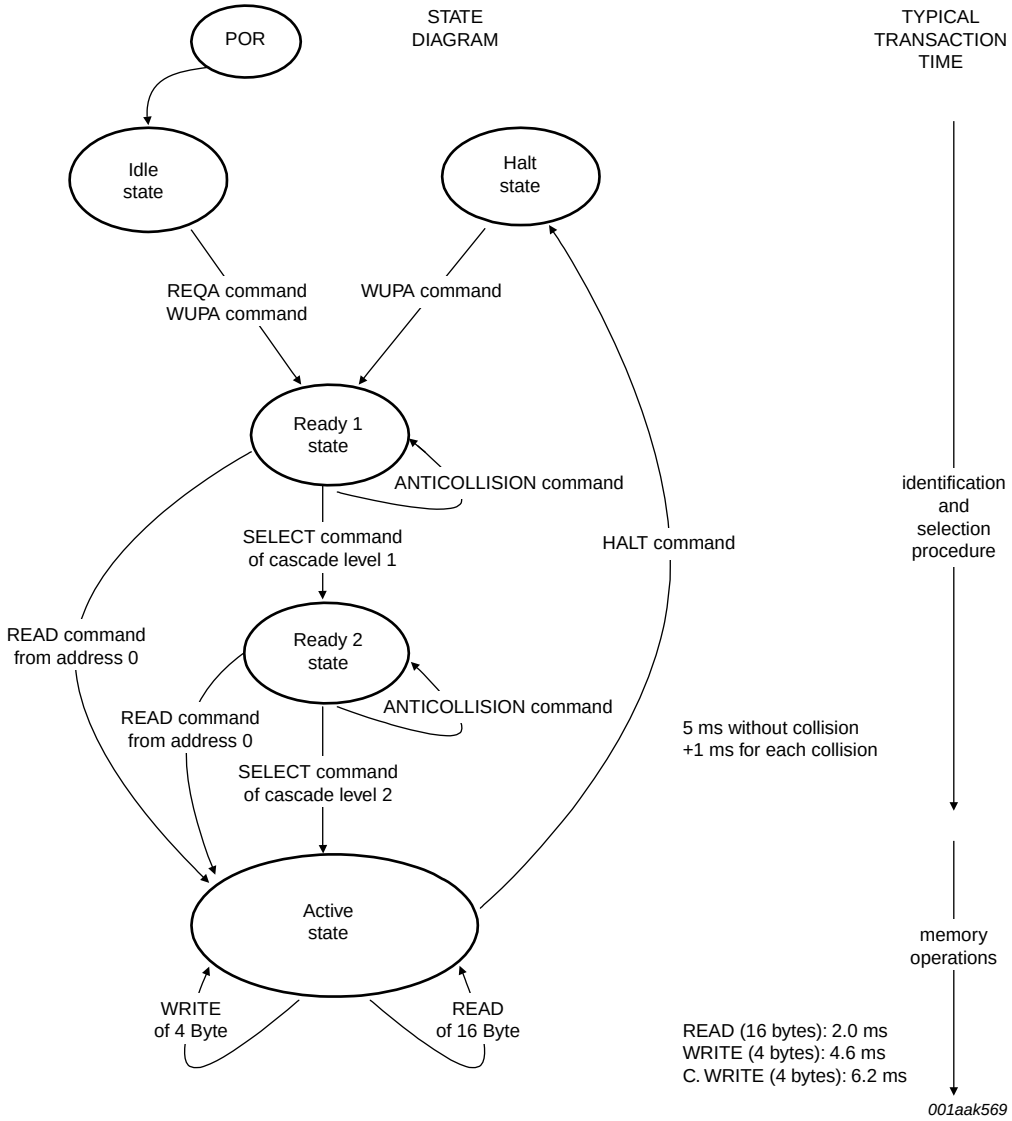
Along with the memory, NTAG203F contains the RF-Interface and the Digital Control Unit. Energy and data are transferred via an antenna, which consists of a coil with a few turns directly connected to the LA and LB of the NTAG203F (see Section 5 for details). No further external components are necessary. (For details on antenna design please refer to the document Ref. 6 “AN11276 NTAG Antenna Design Guide”.)

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7.2 State diagram and logical states description

Commands are initiated by the NFC device and controlled by the NTAG203F command interpreter. This processes the internal states and generates the appropriate response.



In all states, the command interpreter will return to the idle state on receipt of an unexpected command. If the IC was previously in the halt state, it will return to that state.

Fig 4. Communication principle state diagram - 4-byte; 16-byte

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7.2.1 Idle state

After a Power-On Reset (POR), the NTAG203F switches directly to the idle state. It only exits this state when a REQA or a WUPA command is received from the NFC device. Any other data received while in the idle state is interpreted as an error and the NTAG203F remains Idle.

After a correctly executed HALT command, the halt state changes to the wait state which can be exited with a WUPA command.

7.2.2 Ready1 state

In this state, the NTAG203F supports the NFC device when resolving the first part of its UID (3 bytes) with the ANTICOLLISION or SELECT command from cascade level 1. This state is exited correctly after execution of either of the following commands:

- SELECT command from cascade level 1: the NFC device switches NTAG203F into Ready2 state where the second part of the UID is resolved.
- READ command (from address 0): all anticollision mechanisms are bypassed and NTAG203F switches directly to the active state.

Remark: If more than one NTAG203F is in the NFC device field, a READ command from address 0 causes a collision due to the different serial numbers and all NTAG203F devices are selected. Any other data received in the Ready1 state is interpreted as an error and depending on its previous state the NTAG203F returns to the wait, idle or halt state.

7.2.3 Ready2 state

In this state, the NTAG203F supports the NFC device when resolving the second part of its UID (4 bytes) with the cascade level 2 ANTICOLLISION command. This state is usually exited using the cascade level 2 SELECT command.

Alternatively, state Ready2 may be skipped using a READ command (from address 0) as described in state Ready1.

Remark: If more than one NTAG203F is in the NFC device field, a READ command from address 0 causes a collision due to the different serial numbers and all NTAG203F devices are selected. The response of the NTAG203F to the cascade level 2 SELECT command is the Select Acknowledge (SAK) byte. In accordance with ISO/IEC 14443 this byte indicates if the anticollision cascade procedure has finished. The NTAG203F is now uniquely selected and only this device will communicate with the NFC device even when other contactless devices are present in the NFC device field. Any other data received when the device is in this state is interpreted as an error and depending on its previous state the NTAG203F returns to the wait, idle or halt state.

7.2.4 Active state

In the active state either a 16-byte READ or 4-byte WRITE command can be performed. The HALT command exits either the READ or WRITE commands in their active state. Any other data received when the device is in this state is interpreted as an error and depending on its previous state the NTAG203F returns to the wait, idle or halt state.

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7.2.5 Halt state

The halt and idle states constitute the second wait state implemented in the NTAG203F. An already processed NTAG203F can be set into the halt state using the HALT command. In the anticollision phase, this state helps the NFC device to distinguish between processed tags and tags yet to be selected. The NTAG203F can only exit this state on execution of the WUPA command. Any other data received when the device is in this state is interpreted as an error and the NTAG203F state is unchanged. Refer to the document MIFARE collection of currently available application notes for correct implementation of an anticollision procedure based on the idle and halt states and the REQA and WUPA commands.

7.3 Data integrity

The following mechanisms are implemented in the contactless communication link between NFC device and NTAG203F to ensure a reliable data transmission:

- 16 bits CRC per block
- Parity bit for each byte
- Bit count checking
- Bit coding to distinguish between "1", "0", and no information
- Channel monitoring (protocol sequence and bit stream analysis)

7.4 RF interface

The RF-interface is according to the standard for contactless smart cards ISO/IEC 14443A (see Ref. 1).

The RF-field from the NFC device is always present (with short modulation pulses when transmitting data), because it is used for the power supply of the tag.

For both directions of data communication there is one start bit at the beginning of each frame. Each byte is transmitted with a parity bit (odd parity) at the end. The LS Bit of the byte with the lowest address of the selected block is transmitted first. The maximum frame length is 164 bits (16 data bytes + 2 CRC bytes = 16 * 9 + 2 * 9 + 1 start bit + 1 end bit).

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7.5 Memory organization

The 168 bytes of the total EEPROM memory are organized in 42 pages each 4 bytes. 144 bytes (36 pages) are available for the user defined data. Each page contains 4 bytes (32 bits).

Table 5. Memory organization

Page address		Byte number			
Decimal	**Hex**	**0**	**1**	**2**	**3**
0	00h	serial number			
1	01h	serial number			
2	02h	serial number	internal	Lock byte 0	Lock byte 1
3	03h	Capability Container (CC)			
4 to 39	04h to 27h	user memory	user memory	user memory	user memory
40	28h	Lock byte 2	Lock byte 3	-	-
41	29h	16-bit counter	16-bit counter	-	-

7.5.1 UID/serial number

The unique 7 byte serial number (UID) and its two Block Check Character Bytes (BCC) are programmed into the first 9 bytes of the memory. It therefore covers page 00h, page 01h and the first byte of page 02h. The second byte of page 02h is reserved for internal data. Due to security and system requirements these bytes are write-protected after the programming during the IC production.

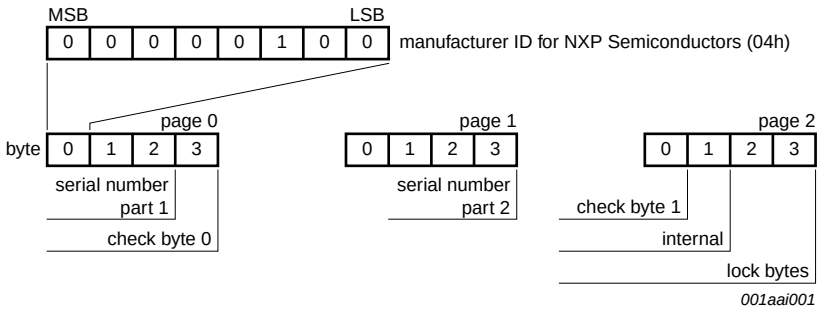


Fig 5. UID/serial number

According to ISO/IEC 14443-3 BCC0 is defined as CT ⊕ SN0 ⊕ SN1 ⊕ SN2. Abbreviations CT stays for Cascade Tag byte (88h) and BCC1 is defined as SN3 ⊕ SN4 ⊕ SN5 ⊕ SN6.

SN0 holds the Manufacturer ID for NXP (04h) according to ISO/IEC 14443-3 and ISO/IEC 7816-6 AMD.1.

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7.5.2 Lock bytes

Lock bytes enable the user to lock parts of the complete memory area for writing. A Read from user memory area cannot be restricted via lock bytes functionality.

The lock bytes functionality is enabled with a WRITE command (see Section 7.9.7 “WRITE”) or COMPATIBILITY WRITE command (see Section 7.9.8 “COMPATIBILITY WRITE”), where 2 out of 4 bytes transmitted are used for setting the lock bytes. Two corresponding bytes - either bytes 2 and 3 for page 02h or bytes 0 and 1 for page 28h - and the actual content of the lock bytes are bit-wise “OR-ed”. The result of OR operation becomes the new content of the lock bytes. Two unused bytes do not have to be considered. Although included in the COMPATIBILITY WRITE or WRITE command, they are ignored when programming the memory.

Table 6. Lock bytes

Name	Page		Function
	Number	Address	
Lock byte 0	2	02h	page and block locking
Lock byte 1	2	02h	page locking
Lock byte 2	40	28h	page and block locking
Lock byte 3	40	28h	functionality and block locking

Due to the built-in bitwise OR operation, this process is irreversible. If a bit is set to “1”, it cannot be changed back to “0” again. Therefore, before locking the lock bytes, the user must ensure that the corresponding user memory area and/or configuration bytes are correctly written.

The configuration written in the lock bytes is active upon the next REQA or WUPA command.

The single bits of the 4 bytes available for locking incorporate 3 different functions:

- the read-only locking of the single pages or blocks of the user memory area
- the read-only locking of the single bytes of the configuration memory area
- the locking of the lock bits themselves

The mapping of single bits to memory area for the first 64 bytes (512 bits) is shown in Figure 6.

The bits of byte 2 and 3 of page 02h represent the field-programmable read-only locking mechanism. Each page from 03h (OTP bits) to 0Fh may be locked individually to prevent further write access by setting the corresponding locking bit Lx to 1. After locking the page is read-only memory.

The 3 least significant bits of lock byte 0 of page 2 are the block-locking bits. Bit 2 handles pages 0Fh to 0Ah, bit 1 pages 09h to 04h and bit 0 page 03h (OTP bits). Once the block locking bits are set, the locking configuration for the corresponding memory area is frozen.

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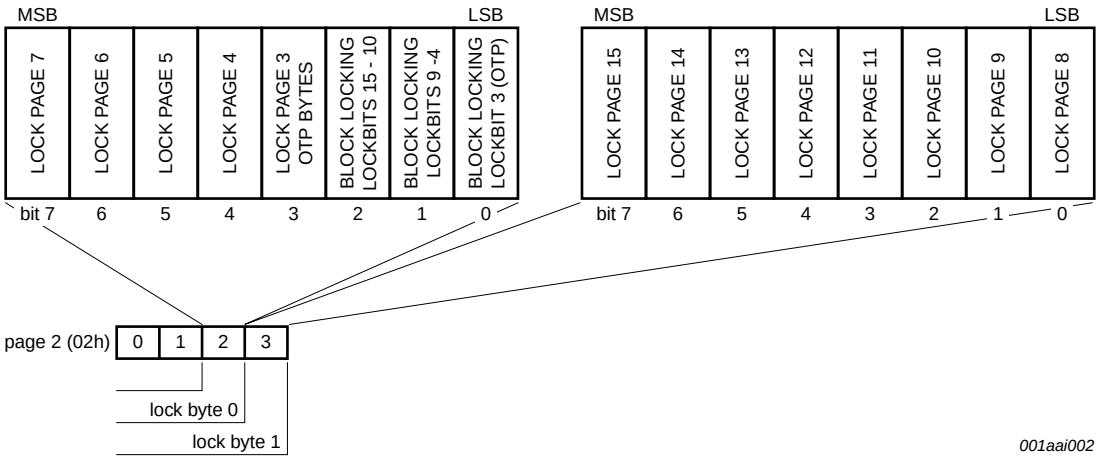


Fig 6. Lock bytes 0 and 1

For locking of pages starting at page address 10h onwards, lock bytes located in page 28h are used. Those two lock bytes cover the memory area of 96 data bytes together with configuration area from page address 28h onwards. Therefore, the granularity is larger then for the first 64 bytes as shown in Figure 7 “Lock bytes 2 and 3”.

The functionality beyond page address 28h which can be locked read-only is:

- the counter
- the lock bytes themselves

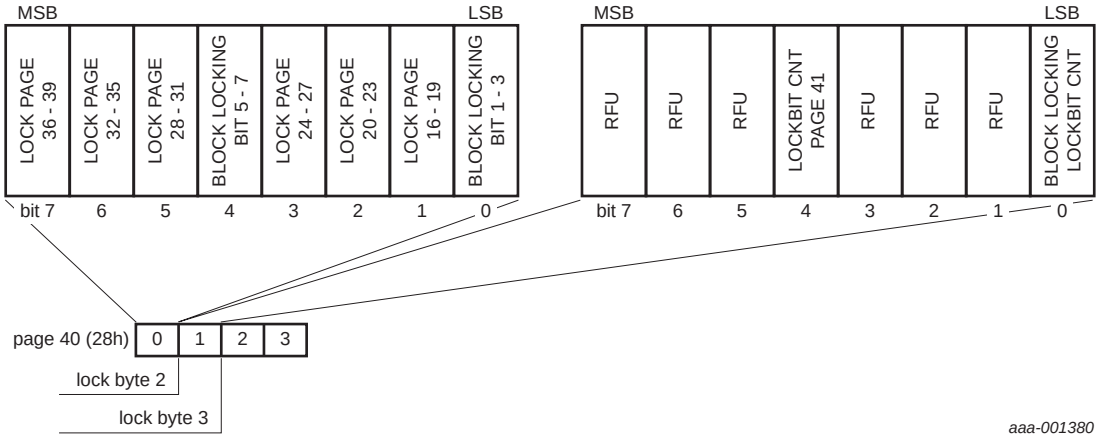


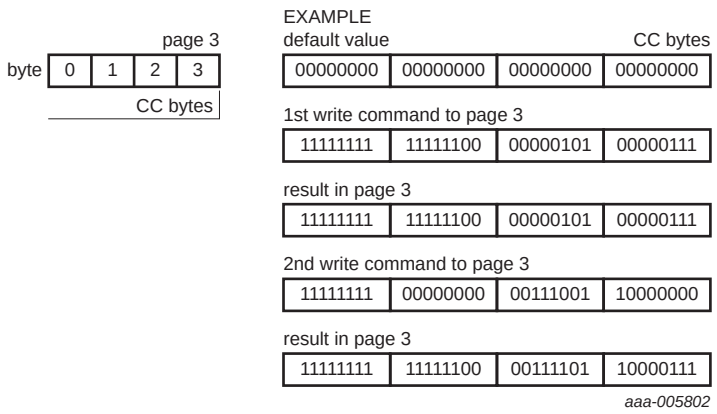
Fig 7. Lock bytes 2 and 3

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7.5.3 Capability Container (CC)

The Capability Container CC (page 3) is programmed during the IC production according to the NFC Forum Type 2 Tag specification Ref. 8. These bytes may be bit-wise modified by a WRITE command.



(1) **Remark:** This memory area may be used as a 32 ticks one-time counter.

Fig 8. CC bytes

The bytes of the WRITE command and the current contents of the CC bytes are bit-wise "OR-ed" and the result becomes the new content of the CC bytes. This process is irreversible. If a bit is set to "1", it cannot be changed back to "0" again.

7.5.4 Data pages

NTAG203F features 144 bytes of data memory. The address range from page 04h to 27h constitutes the read/write area.

Initial state of each byte in the user area is 00h.

A write access to data memory is achieved with WRITE (see Section 7.9.7 "WRITE") or COMPATIBILITY WRITE (see Section 7.9.8 "COMPATIBILITY WRITE") command. In both cases, 4 bytes of memory (one page) will be overwritten. Write access to data memory can be permanently restricted via lock bytes (see Section 7.5.2 "Lock bytes").

NFC Forum Type 2 Tag compliance

NTAG203F has been designed to be compliant with NFC Forum Type 2 Tag specification (see also Ref. 5 "AN1303 Ultralight as Type 2 Tag"). With its 144 bytes of data memory, it can easily support use cases like connection handover, Bluetooth simple pairing, Wi-Fi Protected set-up, device authentication, gaming and others.

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7.5.5 Initial memory configuration

The memory configuration of NTAG203F in delivery state is shown in Table 7 “Initial memory organization”:

Table 7. Initial memory organization

Page address		Byte number			
dec.	**hex.**	**0**	**1**	**2**	**3**
0	00h	UID0	UID1	UID2	BCC0
1	01h	UID3	UID4	UID5	UID6
2	02h	BCC1	internal	00h	00h
3	03h	E1h	10h	12h	00h
4	04h	01h	03h	A0h	10h
5	05h	44h	03h	00h	FEh
6 to 39	06h to 27h	00h	00h	00h	00h
40	28h	00h	00h	rfu	rfu
41	29h	00h	00h	rfu	rfu

The memory configuration in pages 3 to 5 ensures that NTAG203F is a NFC forum Type 2 Tag in INITIALIZED state according to the NFC Forum Technical Specification, Ref. 8 “NFC Forum Tag 2 Type Operation, Technical Specification”. It is recommended that any further modification of the memory pages 2 to 40 should be according to the Ref. 8 “NFC Forum Tag 2 Type Operation, Technical Specification”.

All lock bytes are set to zero meaning that no page or functionality is locked. Counter is set to zero.

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7.6 Counter

NTAG203F features 16-bit one-way counter, located at first two bytes of page 29h. In its delivery state, counter value is set to 0000h.

The first[1] valid Write or Compatibility write to the address 29h can be performed with any value in the range between 0001h and FFFFh and corresponds to initial counter value. Every consequent valid WRITE command, which represents the increment, can contain values between 0001h and 000Fh. Upon such WRITE command and following mandatory RF reset, the value written to the address 29h is added to the counter content.

If - after initial write - a value higher than 000Fh is used as a parameter, NTAG203F will answer with NAK. Once counter value reaches FFFFh and an increment is performed via valid command, NTAG203F will answer with NAK. If the sum of counter value and increment is higher than FFFFh, NTAG203F will answer with NAK and will not update the counter.

Increment by zero (00h) is always possible, but does not have any impact to counter value.

7.7 Tag response to a command from NFC device

NFC Tag Type 2 compliant IC uses, apart from the responses defined in the following sections, two half-byte answers to acknowledge the command received in Active state (see Figure 4 “Communication principle state diagram - 4-byte; 16-byte”).

NFC Tag Type 2 compliant IC distinguishes between positive (ACK) and negative (NAK) acknowledge. Valid values for ACK and NAK are shown in Table 8 “ACK and NAK values”.

Table 8. ACK and NAK values

Answer value	Answer explanation
Ah	positive acknowledge (ACK)
1h	parity or CRC error (NAK)
0h	any other error (NAK)

After every NAK, NTAG203F will perform an internal reset.

7.8 NFC Forum Device timings requirements

For all READ (Section 7.9.5) and WRITE (Section 7.9.7) timings for the NFC device see section 9 of the NFC Digital Protocol, Technical Specification, Version 1.0 (see Ref. 12).

1. First valid write is defined as write to a counter value of zero with an argument different then zero

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7.9 Command set

The ATQA and SAK are identical as for MIFARE Ultralight (see Ref. 7 “MF0ICU1 Functional specification MIFARE Ultralight”). For information on ISO 14443 card activation, see Ref. 3 “AN10834 MIFARE ISO/IEC 14443 PICC Selection”. Summary of data relevant for device identification is given in Section 7.10 “Summary of relevant data for device identification”.

The NTAG203F comprises the command set as described in following chapters.

7.9.1 REQA

Table 9. REQA

Code	Parameter	Data	Integrity mechanism	Response
26h (7-bit)	-	-	Parity	0044h

Description: The NTAG203F accepts the REQA command in Idle state only. The response is the 2-byte ATQA (0044h). REQA and ATQA are implemented fully according to ISO/IEC 14443-3.



Remark: Time units are not to scale and rounded off to 10 µs

Fig 9. REQA

7.9.2 WUPA

Table 10. WUPA

Code	Parameter	Data	Integrity mechanism	Response
52h (7-bit)	-	-	Parity	0044h

Description: NTAG203F accepts the WUPA command in the Idle and Halt state only. The response is the 2-byte ATQA (0044h). WUPA is implemented fully according to ISO/IEC 14443-3.



Remark: Time units are not to scale and rounded off to 10 µs

Fig 10. WUPA

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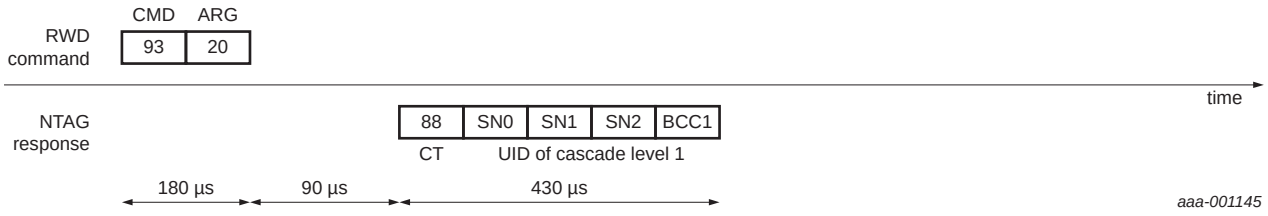
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7.9.3 ANTICOLLISION and SELECT of cascade level 1

Table 11. ANTICOLLISION and SELECT of cascade level 1

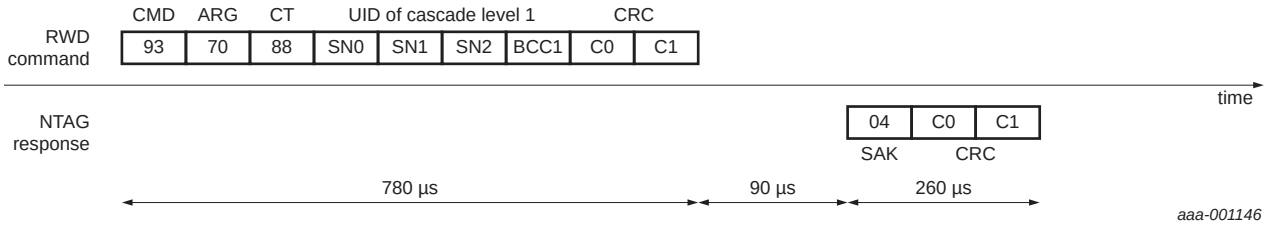
Code	Parameter	Data	Integrity mechanism	Response
Anticollision: 93h	20h	-	Parity, BCC	-
Anticollision: 93h	21h to 67h	Part of the UID	Parity, BCC	Parts of UID
Select: 93h	70h	First 3 bytes of UID	Parity, BCC, CRC	SAK ('04')

Description: The ANTICOLLISION and SELECT commands are based on the same command code. They differ only in the Parameter byte. This byte is per definition 70h in case of SELECT. NTAG203F accepts these commands in the Ready1 state only. The response is part 1 of the UID. Even with incorrect CRC value, the SELECT command will be fully functional.



Remark: Time units are not to scale and rounded off to 10 µs

Fig 11. ANTICOLLISION of cascade level 1



Remark: Time units are not to scale and rounded off to 10 µs

Fig 12. SELECT of cascade level 1

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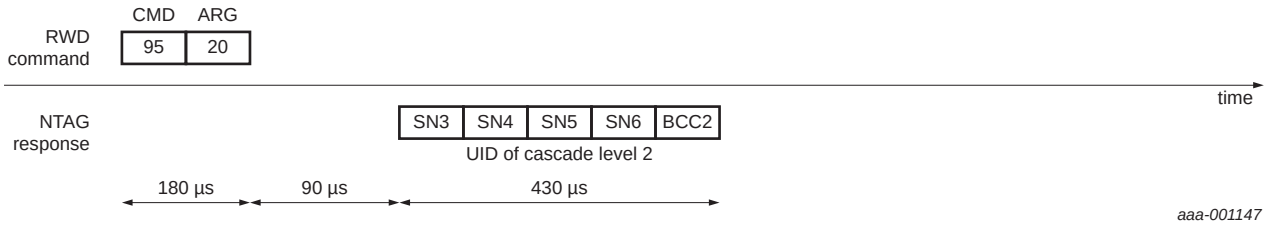
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7.9.4 ANTICOLLISION and SELECT of cascade level 2

Table 12. ANTICOLLISION and SELECT of cascade level 2

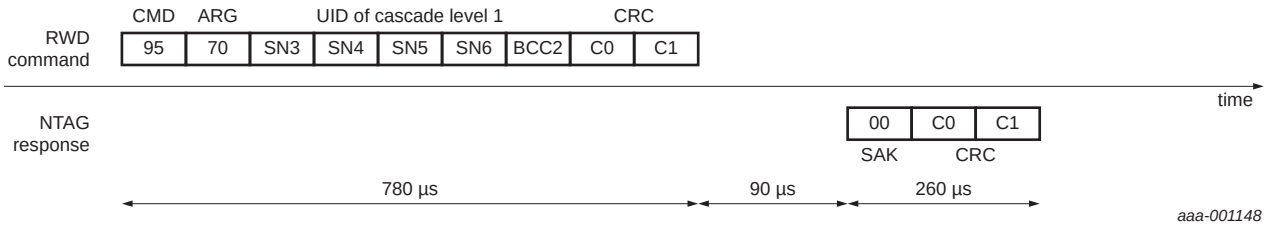
Code	Parameter	Data	Integrity mechanism	Response
Anticollision: 95h	20h	-	Parity, BCC	-
Anticollision: 95h	21h to 67h	Part of the UID	Parity, BCC	Parts of UID
Select: 95h	70h	Second 4 bytes of UID	Parity, BCC, CRC	SAK ('00')

Description: The ANTICOLLISION and SELECT commands are based on the same command code. They differ only in the parameter byte. This byte is per definition 70h in case of SELECT. NTAG203F accepts these commands in the Ready2 state only. The response is part 2 of the UID. Even with incorrect CRC value, the SELECT command will be fully functional.



Remark: Time units are not to scale and rounded off to 10 µs

Fig 13. ANTICOLLISION of cascade level 2



Remark: Time units are not to scale and rounded off to 10 µs

Fig 14. SELECT of cascade level 2

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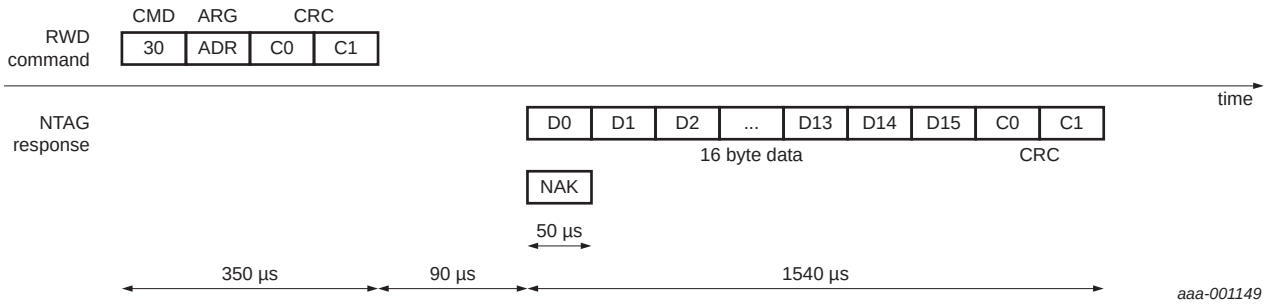
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7.9.5 READ

Table 13. READ

Code	Parameter/ARG	Data	Integrity mechanism	Response
30h	ADR: ‘00h’ to ‘29h‘	-	Parity, CRC	16 Byte Date

Description: The READ command needs the page address as a parameter. Only addresses 00h to 29h are decoded. For higher addresses, NTAG203F returns a NAK. The NTAG203F responds to the READ command by sending 16 bytes starting from the page address defined in the command (e.g. if ADR is ‘03h‘ pages 03h, 04h, 05h, 06h are returned. If ADR is ‘29h’, the contents of pages 29h, 00h, 01h and 02h is returned).



Remark: Time units are not to scale and rounded off to 10 µs

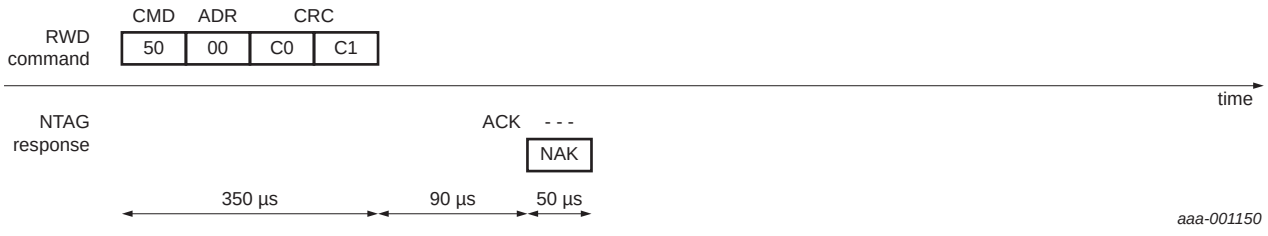
Fig 15. READ

7.9.6 HALT

Table 14. HALT

Code	Parameter	Data	Integrity mechanism	Response
50h	00h	-	Parity, CRC	Passive ACK, NAK

Description: The HALT command is used to set already processed NTAG203F devices into a different waiting state (Halt instead of Idle), which allows a simple separation between devices whose UIDs are already known (as they have already passed the anticollision procedure) and devices that have not yet been identified by their UIDs. This mechanism is a very efficient way of finding all contactless devices in the field of a NFC device. Even with incorrect parity value, the HALT command will be fully functional.



Remark: Time units are not to scale and rounded off to 10 µs

Fig 16. HALT

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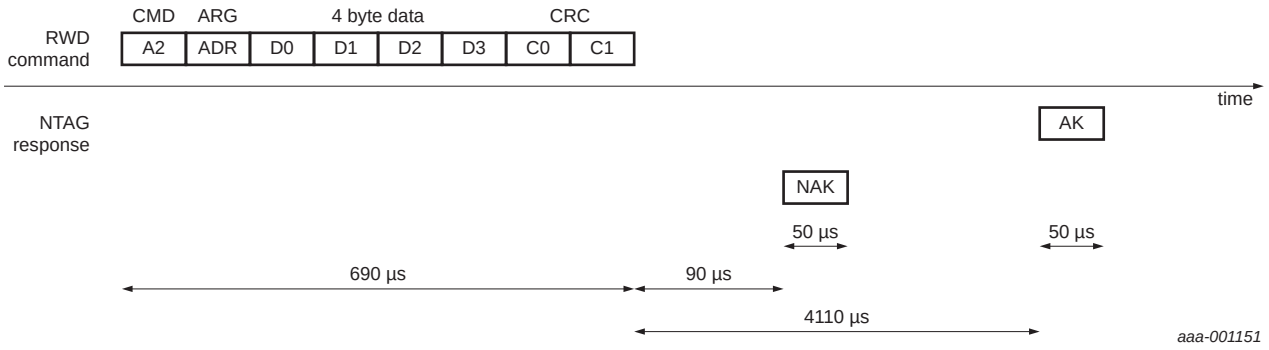
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7.9.7 WRITE

Table 15. WRITE

Code	Parameter/ARG	Data	Integrity mechanism	Response
A2h	ADR: ‘02h’ to ‘29h’	4 Byte	Parity, CRC	ACK or NAK

Description: The WRITE command is used to program the lock bytes in page 02h, the CC bytes in page 03h or the data bytes in pages 04h to 05h. A WRITE command is performed page-wise, programming 4 bytes in a page.



Remark: Time units are not to scale and rounded off to 10 µs

Fig 17. WRITE

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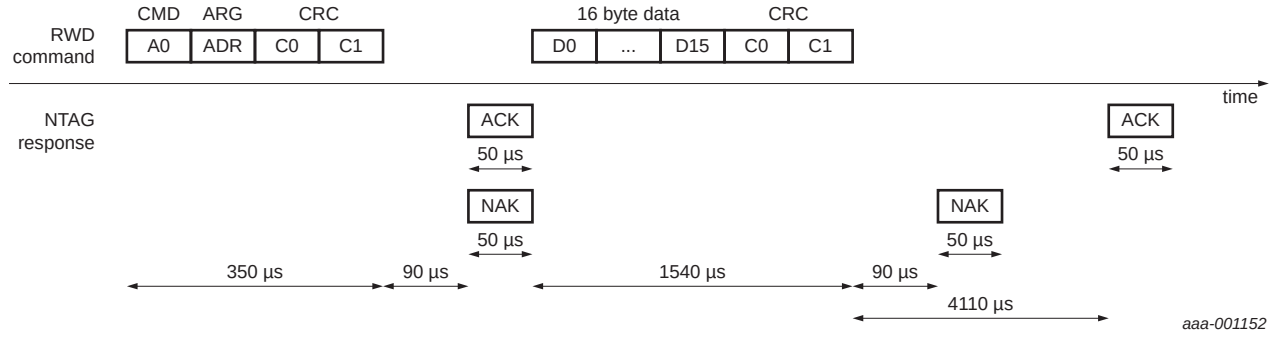
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7.9.8 COMPATIBILITY WRITE

Table 16. COMPATIBILITY WRITE

Code	Parameter/ARG	Data	Integrity mechanism	Response
A0h	ADR: '02h' to '29h'	16 Byte	Parity, CRC	ACK or NAK

Description: The COMPATIBILITY WRITE command was implemented to accommodate the established NFC device infrastructure. Even though 16 bytes are transferred to the NTAG203F, only the least significant 4 bytes (bytes D0 to D3) will be written to the specified address. It is recommended to set the remaining bytes D4 to D15 to all '0'.



Remark: Time units are not to scale and rounded off to 10 µs

Fig 18. COMPATIBILITY WRITE

REMARK: The timings in Fig.19 are typical timings. The NFC forum device must respect the following minimum timings and maximum timeouts.

Table 17. COMPATIBILITY_WRITE timing

These times exclude the end of communication of the NFC Forum device.

	T_{ACK} min	T_{ACK} max	T_{NAK} min	T_{NAK} max	$T_{TimeOut}$
COMPATIBILITY_WRITE 1st ACK/NAK	71 µs	$T_{TimeOut}$	71 µs	$T_{TimeOut}$	5 ms
COMPATIBILITY_WRITE 2nd ACK/NAK	71 µs	$T_{TimeOut}$	71 µs	$T_{TimeOut}$	10 ms

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7.10 Summary of relevant data for device identification

Table 18. Summary of relevant data for device identification

Code	Type	Value	Binary Format	Remark
ATQA	2 Byte	0044h	0000 0000 0100 0100 1st '1' indicates cascade level 2 2nd '1' indicates family	OK
CT	1 Byte Cascade Tag	88h	1000 1000 ensures collision with cascade level 1 products	Hard Coded
SAK (casc. level 1)	1 Byte	04h	0000 0100 '1' indicates additional cascade level	OK
SAK (casc. level 2)	1 Byte	00h	0000 0000 indicates complete UID and NTAG203F functionality	OK
Manufacturer Byte	1 Byte	04h	0000 0100 indicates manufacturer NXP	Acc. to ISO/IEC 14443-3 and ISO/IEC 7816-6 AMD.1

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8. Limiting values

Table 19. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).[1][2]

Symbol	Parameter	Conditions		Min	Max	Unit
I_I	input current			-	30	mA
I_{load}	load current	FD-V_{SS}	[4]	-	10	µA
T_{stg}	storage temperature			–55	+125	°C
V_{ESD}	electrostatic discharge voltage	measured on pin LA-LB	[3]	2	-	kV

[1] Stresses above one or more of the limiting values may cause permanent damage to the device.

[2] Exposure to limiting values for extended periods may affect device reliability.

[3] MIL Standard 883-C method 3015; Human body model: C = 100 pF, R = 1.5 kΩ.

[4] For safe operation the suggested maximum static current from the VDD pin shall not be above the maximum load current (refer to Application note Ref. 11 “AN11141 How to use the FD pin”).

9. Characteristics

9.1 Electrical characteristics

Table 20. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
f_i	input frequency			-	13.56	-	MHz
C_i	input capacitance	50 pF version	[1]	44	50	56	pF
V_o	output voltage	FD pin		1.2	1.8	2.0	V
T_{amb}	ambient temperature			–25	22	+70	°C
EEPROM characteristics							
$t_{cy(W)}$	write cycle time			-	4.1	-	ms
t_{ret}	retention time	T_{amb} = 22 °C		10	-	-	year
$N_{endu(W)}$	write endurance	T_{amb} = 22 °C		10000	-	-	cycle

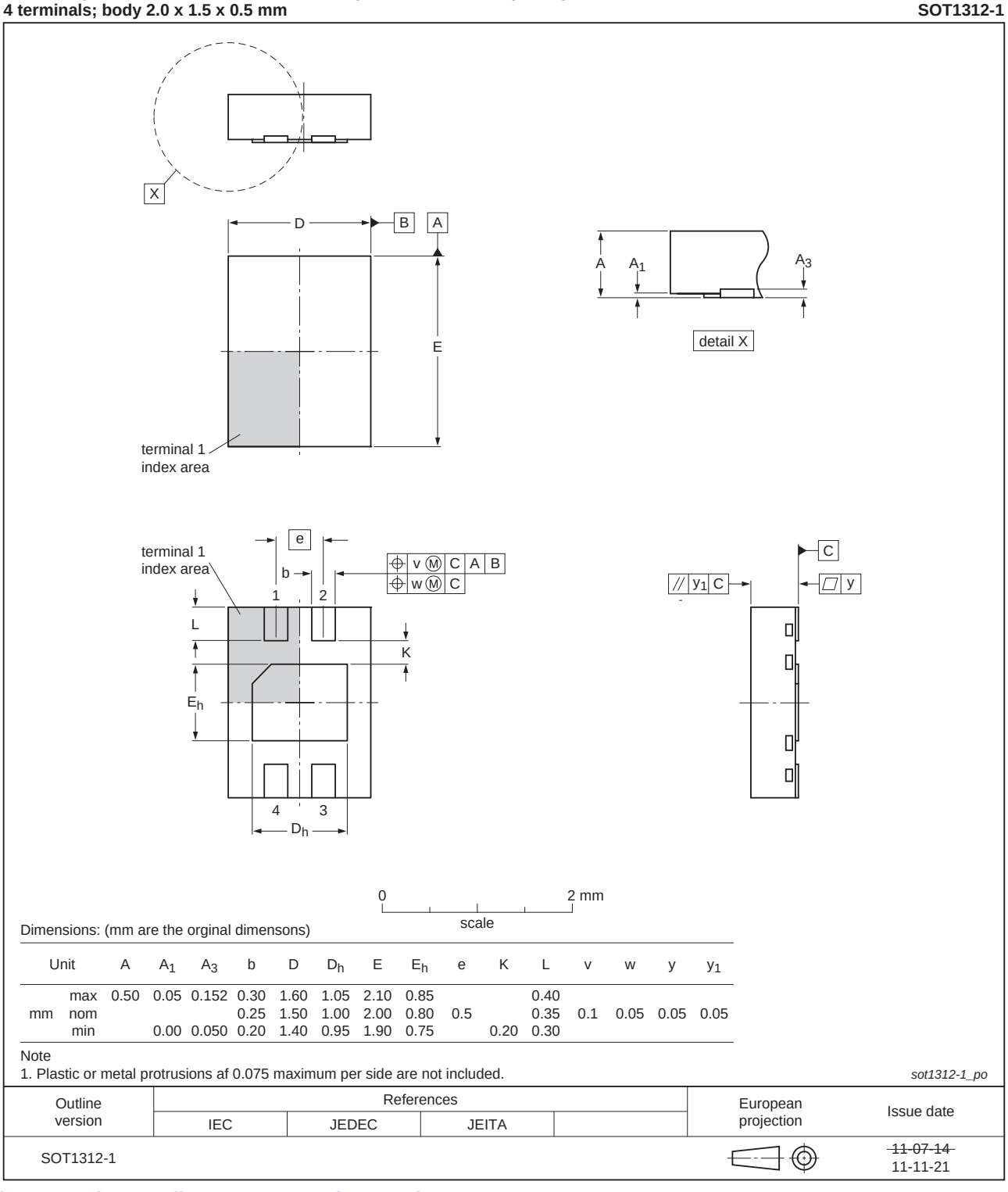
[1] LCR meter HP 4285, T_{amb} = 22 °C, Cp-D, f_i = 13.56 MHz, 2Veff.

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10. Package outline

HXSON4: plastic thermal enhanced extremely thin small outline package; no leads; 4 terminals; body 2.0 x 1.5 x 0.5 mm **SOT1312-1**



Dimensions: (mm are the orginal dimensons)

Unit		A	A_1	A_3	b	D	D_h	E	E_h	e	K	L	v	w	y	y_1
	max	0.50	0.05	0.152	0.30	1.60	1.05	2.10	0.85			0.40				
mm	nom				0.25	1.50	1.00	2.00	0.80	0.5		0.35	0.1	0.05	0.05	0.05
	min		0.00	0.050	0.20	1.40	0.95	1.90	0.75		0.20	0.30				

Note

1. Plastic or metal protrusions af 0.075 maximum per side are not included.

sot1312-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1312-1						~~11-07-14~~ 11-11-21

Fig 19. Package outline SOT1312AB2 (HXSON4)

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11. Abbreviations

Table 21. Abbreviations

Acronym	Description
ACK	positive ACKnowledge
ATQA	Answer To reQuest, type A
BCC	Block Check Characters byte
CBC	Cipher-Block Chaining
CC	Capability Container
CRC	Cyclic Redundancy Check
CT	Cascade Tag, Type A
EEPROM	Electrically Erasable Programmable Read-Only Memory
IV	Initial Value
MSB	Most Significant Bit
NAK	Negative AcKnowledge
LSB	Least Significant Bit
OTP	One Time Programmable
Passive ACK	Implicit acknowledge without PICC answer
PCD	Proximity Coupling Device
PICC	Proximity Integrated Circuit Card
POR	Power On Reset
REQA	ReQuest Answer, type A
RF	Radio Frequency
SAK	Select AcKnowledge, type A
UID	Unique IDentifier
WUPA	Wake-UP command, type A

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12. References

[1] **ISO/IEC —** 14443-2 (2001) and ISO/IEC 14443-2 (2001)

[2] **AN10833 MIFARE Type Identification Procedure —** Application note, BU-ID Doc. No.: 0184**[2]

[3] **AN10834 MIFARE ISO/IEC 14443 PICC Selection —** Application note, BU-ID Doc. No.: 1308**[2]

[4] **AN Ultralight Features and Hints —** Application note, BU-ID Doc. No.: 0731**[2]

[5] **AN1303 Ultralight as Type 2 Tag —** Application note, BU-ID Doc. No.: 1303**[2]

[6] **AN11276 NTAG Antenna Design Guide —** Application note, BU-ID Doc. No.: 2421**[2]

[7] **MF0ICU1 Functional specification MIFARE Ultralight —** Product data sheet, BU-ID Doc. No. 0286**[2]

[8] **NFC Forum Tag 2 Type Operation, Technical Specification —** NFC Forum, 31.05.2011, Version 1.1

[9] **NFC Data Exchange Format (NDEF), Technical Specification —** NFC Forum, 24.07.2006, Version 1.0

[10] **AN10365 Surface mount reflow soldering —** Application note, NXP Semiconductors

[11] **AN11141 How to use the FD pin —** Application note, BU-ID Doc. No.: 2214*[2]

[12] **NFC Digital Protocol, Technical Specification —** NFC Forum, 17.11.2010, Version 1.0

2. ** ... document version number

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13. Revision history

Table 22. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
NTAG203F v.3.5	20150928	Product data sheet	-	NTAG203F v.3.4
Modifications:	• HWSON8 package discontinued and removed from data sheet • Section 14.4 “Licenses”: updated			
NTAG203F v.3.4	20130910	Product data sheet	-	NTAG203F v.3.3
Modifications:	• Section 3 “Ordering information”: Package description updated			
NTAG203F v.3.3	20130212	Product data sheet	-	NTAG203F v.3.2
Modifications:	• Drawings update			
NTAG203F v.3.2	20130123	Product data sheet	-	NTAG203F v.3.1
Modifications:	• Correction of HXSON4 Marking			
NTAG203F v.3.1	20121113	Product data sheet	-	NTAG203F v.3.0
Modifications:	• Editorial changings and corrections • New package “HXSON4” added • Data retention updated to 10 years • Section 14.4 “Licenses”: updated • Security status changed into “COMPANY PUBLIC”			
NTAG203F v.3.0	20111215	Product data sheet	-	-

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[2] The term 'short data sheet' is explained in section "Definitions".

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