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MUN5211DW1T1 Series

Preferred Devices

Dual Bias Resistor Transistors

NPN Silicon Surface Mount Transistors with Monolithic Bias Resistor Network

The BRT (Bias Resistor Transistor) contains a single transistor with a monolithic bias network consisting of two resistors; a series base resistor and a base−emitter resistor. These digital transistors are designed to replace a single device and its external resistor bias network. The BRT eliminates these individual components by integrating them into a single device. In the MUN5211DW1T1 series, two BRT devices are housed in the SOT−363 package which is ideal for low power surface mount applications where board space is at a premium.

Features

- Simplifies Circuit Design
- Reduces Board Space
- Reduces Component Count
- Pb−Free Packages are Available

MAXIMUM RATINGS

(T_A = 25°C unless otherwise noted, common for Q_1 and Q_2)

Rating	Symbol	Value	Unit
Collector-Base Voltage	V_{CBO}	50	Vdc
Collector-Emitter Voltage	V_{CEO}	50	Vdc
Collector Current	I_C	100	mAdc

THERMAL CHARACTERISTICS

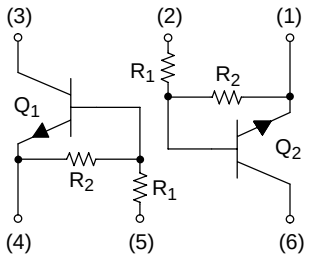
Characteristic (One Junction Heated)	Symbol	Max	Unit
Total Device Dissipation T_A = 25°C Derate above 25°C	P_D	187 (Note 1) 256 (Note 2) 1.5 (Note 1) 2.0 (Note 2)	mW mW/°C
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	670 (Note 1) 490 (Note 2)	°C/W
Characteristic (Both Junctions Heated)	**Symbol**	**Max**	**Unit**
Total Device Dissipation T_A = 25°C Derate above 25°C	P_D	250 (Note 1) 385 (Note 2) 2.0 (Note 1) 3.0 (Note 2)	mW mW/°C
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	493 (Note 1) 325 (Note 2)	°C/W
Thermal Resistance, Junction-to-Lead	$R_{\theta JL}$	188 (Note 1) 208 (Note 2)	°C/W
Junction and Storage Temperature	T_J, T_{stg}	−55 to +150	°C

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

1. FR−4 @ Minimum Pad
2. FR−4 @ 1.0 x 1.0 inch Pad

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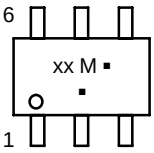
http://onsemi.com





SOT−363
CASE 419B
STYLE 1

MARKING DIAGRAM



xx = Device Code
M = Date Code*
▪ = Pb−Free Package
(Note: Microdot may be in either location)

*Date Code orientation and/or position may vary depending upon manufacturing location.

DEVICE MARKING INFORMATION

See specific marking information in the device marking table on page 2 of this data sheet.

Preferred devices are recommended choices for future use and best overall value.

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DEVICE MARKING AND RESISTOR VALUES

Device	Package	Marking	R1 (K)	R2 (K)	Shipping†
MUN5211DW1T1	SOT−363	7A	10	10	3000/Tape & Reel
MUN5211DW1T1G	SOT−363 (Pb−Free)	7A	10	10	3000/Tape & Reel
MUN5212DW1T1	SOT−363	7B	22	22	3000/Tape & Reel
MUN5212DW1T1G	SOT−363 (Pb−Free)	7B	22	22	3000/Tape & Reel
MUN5213DW1T1	SOT−363	7C	47	47	3000/Tape & Reel
MUN5213DW1T1G	SOT−363 (Pb−Free)	7C	47	47	3000/Tape & Reel
MUN5214DW1T1	SOT−363	7D	10	47	3000/Tape & Reel
MUN5214DW1T1G	SOT−363 (Pb−Free)	7D	10	47	3000/Tape & Reel
MUN5215DW1T1	SOT−363	7E	10	∞	3000/Tape & Reel
MUN5215DW1T1G	SOT−363 (Pb−Free)	7E	10	∞	3000/Tape & Reel
MUN5216DW1T1	SOT−363	7F	4.7	∞	3000/Tape & Reel
MUN5216DW1T1G	SOT−363 (Pb−Free)	7F	4.7	∞	3000/Tape & Reel
MUN5230DW1T1	SOT−363	7G	1.0	1.0	3000/Tape & Reel
MUN5230DW1T1G	SOT−363 (Pb−Free)	7G	1.0	1.0	3000/Tape & Reel
MUN5231DW1T1	SOT−363	7H	2.2	2.2	3000/Tape & Reel
MUN5231DW1T1G	SOT−363 (Pb−Free)	7H	2.2	2.2	3000/Tape & Reel
MUN5232DW1T1	SOT−363	7J	4.7	4.7	3000/Tape & Reel
MUN5232DW1T1G	SOT−363 (Pb−Free)	7J	4.7	4.7	3000/Tape & Reel
MUN5233DW1T1	SOT−363	7K	4.7	47	3000/Tape & Reel
MUN5233DW1T1G	SOT−363 (Pb−Free)	7K	4.7	47	3000/Tape & Reel
MUN5234DW1T1	SOT−363	7L	22	47	3000/Tape & Reel
MUN5234DW1T1G	SOT−363 (Pb−Free)	7L	22	47	3000/Tape & Reel
MUN5235DW1T1	SOT−363	7M	2.2	47	3000/Tape & Reel
MUN5235DW1T1G	SOT−363 (Pb−Free)	7M	2.2	47	3000/Tape & Reel
MUN5236DW1T1	SOT−363	7N	100	100	3000/Tape & Reel
MUN5236DW1T1G	SOT−363 (Pb−Free)	7N	100	100	3000/Tape & Reel
MUN5237DW1T1	SOT−363	7P	47	22	3000/Tape & Reel
MUN5237DW1T1G	SOT−363 (Pb−Free)	7P	47	22	3000/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted, common for Q_1 and Q_2)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Collector-Base Cutoff Current (V_{CB} = 50 V, I_E = 0)		I_{CBO}	–	–	100	nAdc
Collector-Emitter Cutoff Current (V_{CE} = 50 V, I_B = 0)		I_{CEO}	–	–	500	nAdc
Emitter-Base Cutoff Current	MUN5211DW1T1, G	I_{EBO}	–	–	0.5	mAdc
(V_{EB} = 6.0 V, I_C = 0)	MUN5212DW1T1, G		–	–	0.2	
	MUN5213DW1T1, G		–	–	0.1	
	MUN5214DW1T1, G		–	–	0.2	
	MUN5215DW1T1, G		–	–	0.9	
	MUN5216DW1T1, G		–	–	1.9	
	MUN5230DW1T1, G		–	–	4.3	
	MUN5231DW1T1, G		–	–	2.3	
	MUN5232DW1T1, G		–	–	1.5	
	MUN5233DW1T1, G		–	–	0.18	
	MUN5234DW1T1, G		–	–	0.13	
	MUN5235DW1T1, G		–	–	0.2	
	MUN5236DW1T1, G		–	–	0.05	
	MUN5237DW1T1, G		–	–	0.13	
Collector-Base Breakdown Voltage (I_C = 10 μA, I_E = 0)		$V_{(BR)CBO}$	50	–	–	Vdc
Collector-Emitter Breakdown Voltage (Note 3) (I_C = 2.0 mA, I_B = 0)		$V_{(BR)CEO}$	50	–	–	Vdc

3. Pulse Test: Pulse Width < 300 μs, Duty Cycle < 2.0%

ON CHARACTERISTICS (Note 4)

DC Current Gain	MUN5211DW1T1, G	h_{FE}	35	60	–	
(V_{CE} = 10 V, I_C = 5.0 mA)	MUN5212DW1T1, G		60	100	–	
	MUN5213DW1T1, G		80	140	–	
	MUN5214DW1T1, G		80	140	–	
	MUN5215DW1T1, G		160	350	–	
	MUN5216DW1T1, G		160	350	–	
	MUN5230DW1T1, G		3.0	5.0	–	
	MUN5231DW1T1, G		8.0	15	–	
	MUN5232DW1T1, G		15	30	–	
	MUN5233DW1T1, G		80	200	–	
	MUN5234DW1T1, G		80	150	–	
	MUN5235DW1T1, G		80	140	–	
	MUN5236DW1T1, G		80	150	–	
	MUN5237DW1T1, G		80	140	–	

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Collector-Emitter Saturation Voltage		$V_{CE(sat)}$				Vdc
(I_C = 10 mA, I_B = 0.3 mA)	MUN5211DW1T1, G		–	–	0.25	
	MUN5212DW1T1, G		–	–	0.25	
	MUN5213DW1T1, G		–	–	0.25	
	MUN5214DW1T1, G		–	–	0.25	
	MUN5235DW1T1, G		–	–	0.25	
	MUN5236DW1T1, G		–	–	0.25	
(I_C = 10 mA, I_B = 5 mA)	MUN5230DW1T1, G		–	–	0.25	
	MUN5231DW1T1, G		–	–	0.25	
	MUN5237DW1T1, G		–	–	0.25	
(I_C = 10 mA, I_B = 1 mA)	MUN5215DW1T1, G		–	–	0.25	
	MUN5216DW1T1, G		–	–	0.25	
	MUN5232DW1T1, G		–	–	0.25	
	MUN5233DW1T1, G		–	–	0.25	
	MUN5234DW1T1, G		–	–	0.25	
Output Voltage (on)		V_{OL}				Vdc
(V_{CC} = 5.0 V, V_B = 2.5 V, R_L = 1.0 kΩ)	MUN5211DW1T1, G		–	–	0.2	
	MUN5212DW1T1, G		–	–	0.2	
	MUN5214DW1T1, G		–	–	0.2	
	MUN5215DW1T1, G		–	–	0.2	
	MUN5216DW1T1, G		–	–	0.2	
	MUN5230DW1T1, G		–	–	0.2	
	MUN5231DW1T1, G		–	–	0.2	
	MUN5232DW1T1, G		–	–	0.2	
	MUN5233DW1T1, G		–	–	0.2	
	MUN5234DW1T1, G		–	–	0.2	
	MUN5235DW1T1, G		–	–	0.2	
(V_{CC} = 5.0 V, V_B = 3.5 V, R_L = 1.0 kΩ)	MUN5213DW1T1, G		–	–	0.2	
(V_{CC} = 5.0 V, V_B = 5.5 V, R_L = 1.0 kΩ)	MUN5236DW1T1, G		–	–	0.2	
(V_{CC} = 5.0 V, V_B = 4.0 V, R_L = 1.0 kΩ)	MUN5237DW1T1, G		–	–	0.2	

4. Pulse Test: Pulse Width < 300 μs, Duty Cycle < 2.0%

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ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted, common for Q_1 and Q_2) (Continued)

Characteristic		Symbol	Min	Typ	Max	Unit
ON CHARACTERISTICS (Note 5) (Continued)						
Output Voltage (off)		V_{OH}				Vdc
(V_{CC} = 5.0 V, V_B = 0.5 V, R_L = 1.0 kΩ)	MUN5211DW1T1, G		4.9	–	–	
	MUN5212DW1T1, G		4.9	–	–	
	MUN5213DW1T1, G		4.9	–	–	
	MUN5214DW1T1, G		4.9	–	–	
	MUN5233DW1T1, G		4.9	–	–	
	MUN5234DW1T1, G		4.9	–	–	
	MUN5235DW1T1, G		4.9	–	–	
(V_{CC} = 5.0 V, V_B = 0.050 V, R_L = 1.0 kΩ)	MUN5230DW1T1, G		4.9	–	–	
(V_{CC} = 5.0 V, V_B = 0.25 V, R_L = 1.0 kΩ)	MUN5215DW1T1, G		4.9	–	–	
	MUN5216DW1T1, G		4.9	–	–	
	MUN5231DW1T1, G		4.9	–	–	
	MUN5232DW1T1, G		4.9	–	–	
	MUN5236DW1T1, G		4.9	–	–	
	MUN5237DW1T1, G		4.9	–	–	
Input Resistor	MUN5211DW1T1, G	R1	7.0	10	13	k Ω
	MUN5212DW1T1, G		15.4	22	28.6	
	MUN5213DW1T1, G		32.9	47	61.1	
	MUN5214DW1T1, G		7.0	10	13	
	MUN5215DW1T1, G		7.0	10	13	
	MUN5216DW1T1, G		3.3	4.7	6.1	
	MUN5230DW1T1, G		0.7	1.0	1.3	
	MUN5231DW1T1, G		1.5	2.2	2.9	
	MUN5232DW1T1, G		3.3	4.7	6.1	
	MUN5233DW1T1, G		3.3	4.7	6.1	
	MUN5234DW1T1, G		15.4	22	28.6	
	MUN5235DW1T1, G		1.54	2.2	2.86	
	MUN5236DW1T1, G		70	100	130	
	MUN5237DW1T1, G		32.9	47	61.1	
Resistor Ratio	MUN5211DW1T1, G/MUN5212DW1T1, G/	R1/R2				
	MUN5213DW1T1, G/MUN5236DW1T1, G		0.8	1.0	1.2	
	MUN5214DW1T1, G		0.17	0.21	0.25	
	MUN5215DW1T1, G/MUN5216DW1T1, G		–	–	–	
	MUN5230DW1T1, G/MUN5231DW1T1, G/MUN5232DW1T1, G		0.8	1.0	1.2	
	MUN5233DW1T1, G		0.055	0.1	0.185	
	MUN5234DW1T1, G		0.38	0.47	0.56	
	MUN5235DW1T1, G		0.038	0.047	0.056	
	MUN5237DW1T1, G		1.7	2.1	2.6	

5. Pulse Test: Pulse Width < 300 μs, Duty Cycle < 2.0%

ALL MUN5211DW1T1 SERIES DEVICES

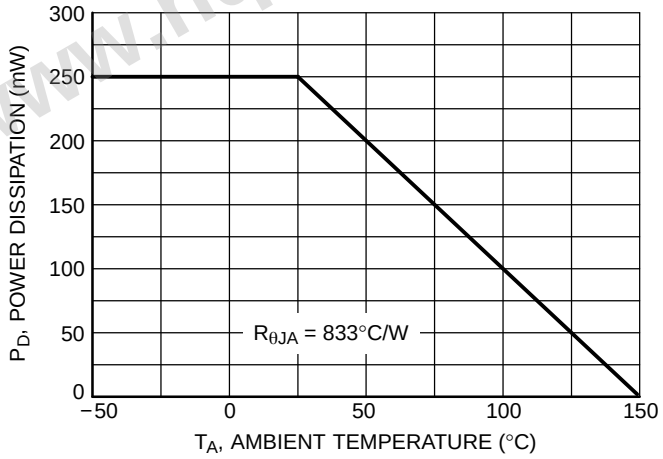


Figure 1. Derating Curve

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TYPICAL ELECTRICAL CHARACTERISTICS — MUN5211DW1T1

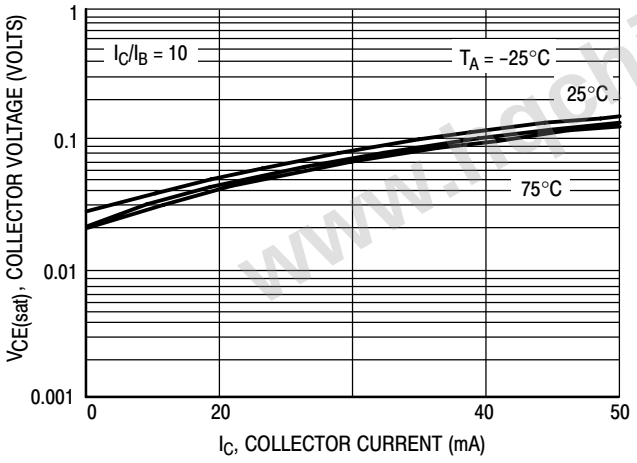


Figure 2. $V_{CE(sat)}$ versus I_C

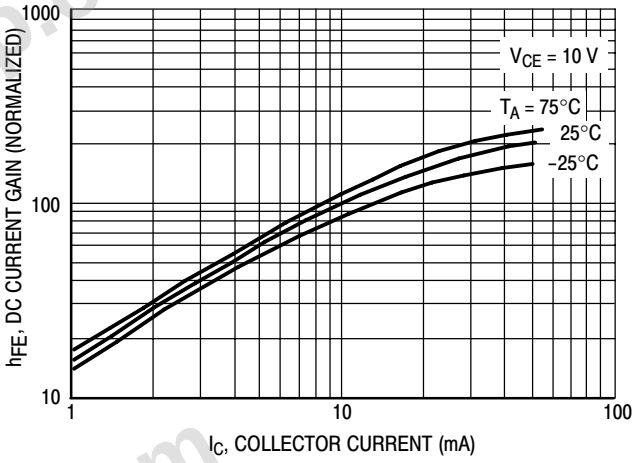


Figure 3. DC Current Gain

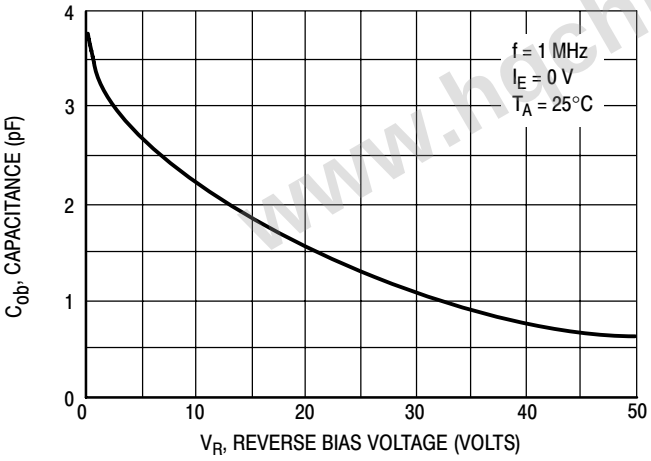


Figure 4. Output Capacitance

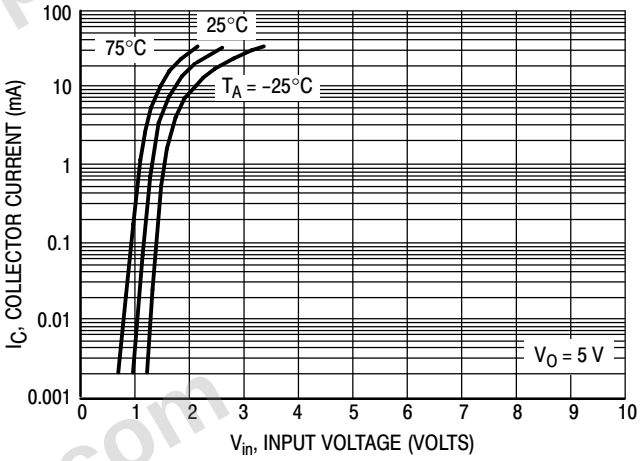


Figure 5. Output Current versus Input Voltage

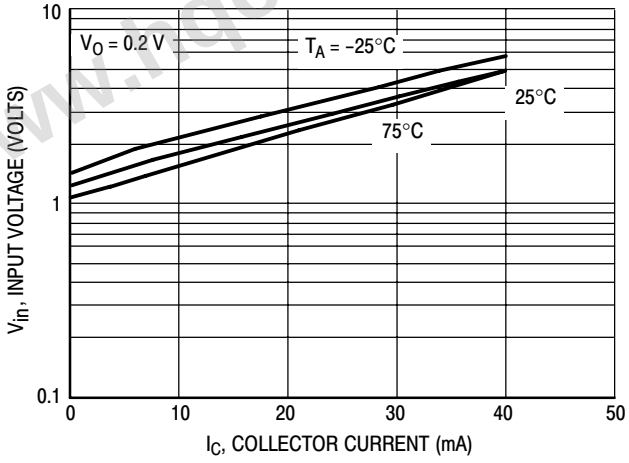


Figure 6. Input Voltage versus Output Current

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TYPICAL ELECTRICAL CHARACTERISTICS — MUN5212DW1T1

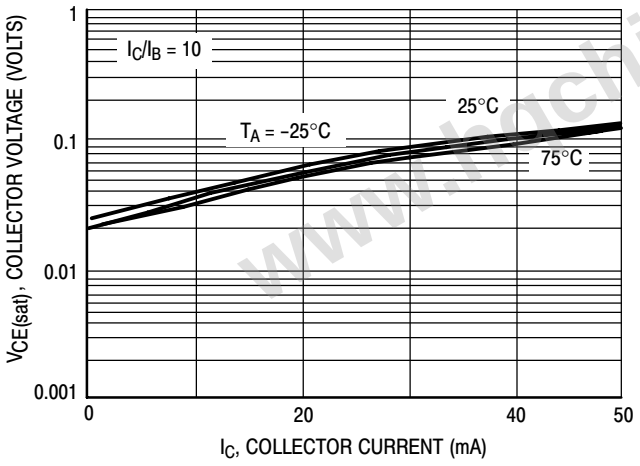


Figure 7. $V_{CE(sat)}$ versus I_C

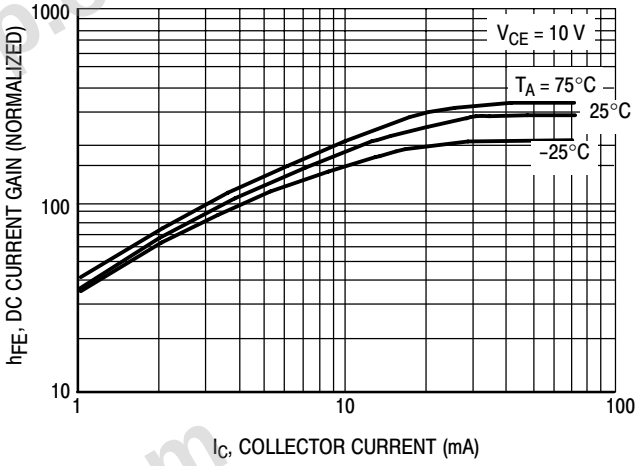


Figure 8. DC Current Gain

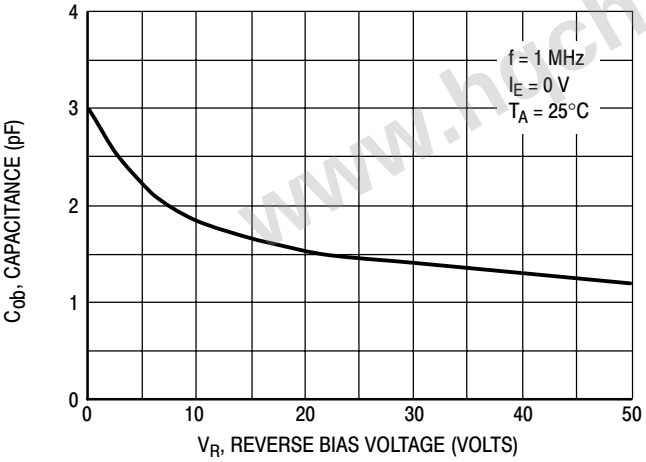


Figure 9. Output Capacitance

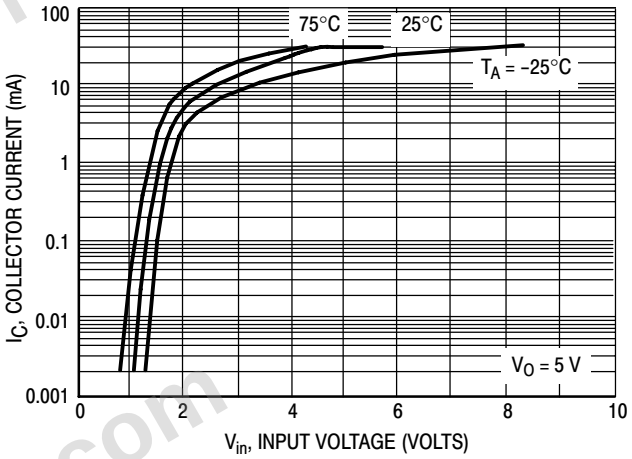


Figure 10. Output Current versus Input Voltage

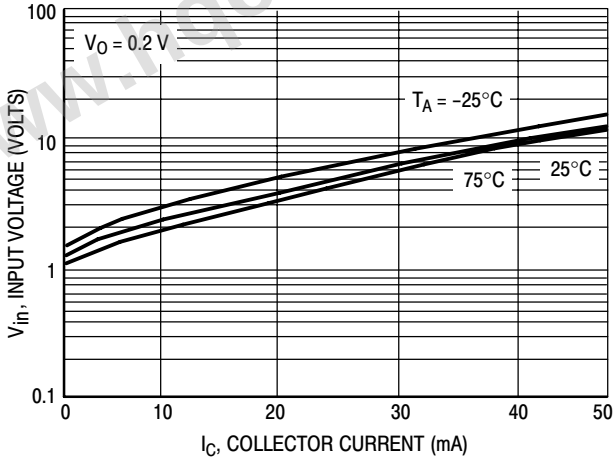


Figure 11. Input Voltage versus Output Current

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TYPICAL ELECTRICAL CHARACTERISTICS — MUN5213DW1T1

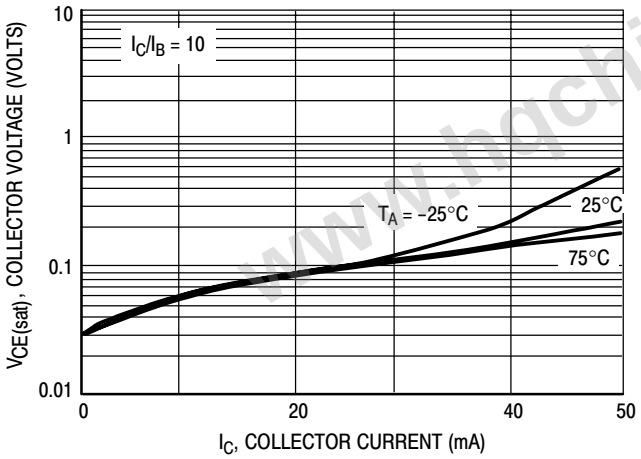


Figure 12. $V_{CE(sat)}$ versus I_C

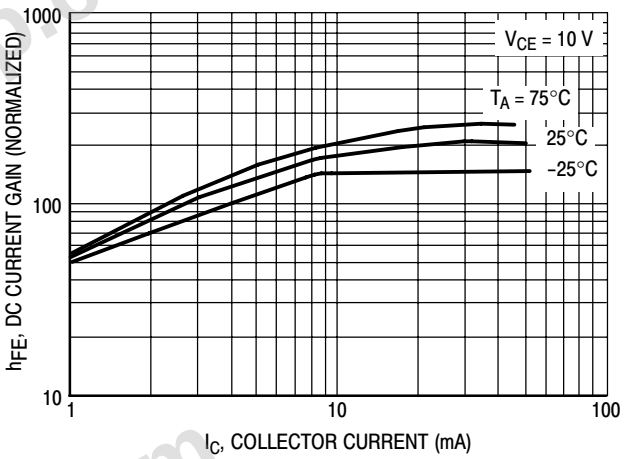


Figure 13. DC Current Gain

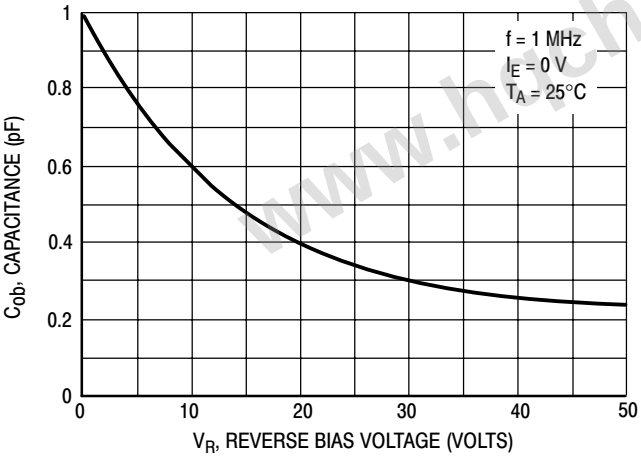


Figure 14. Output Capacitance

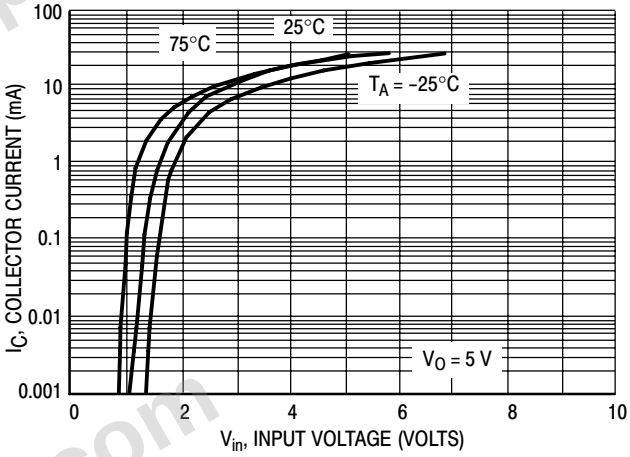


Figure 15. Output Current versus Input Voltage

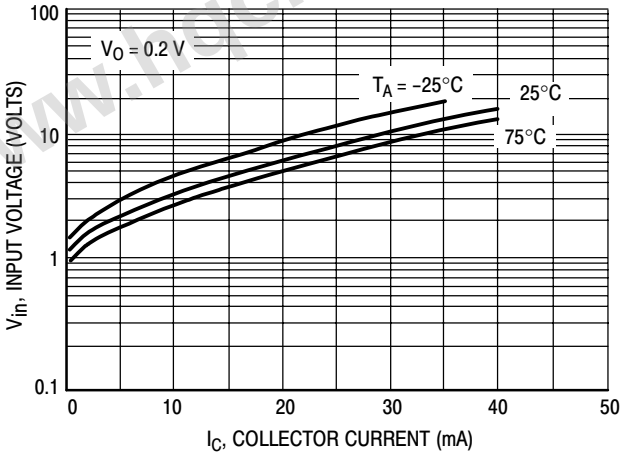


Figure 16. Input Voltage versus Output Current

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TYPICAL ELECTRICAL CHARACTERISTICS — MUN5214DW1T1

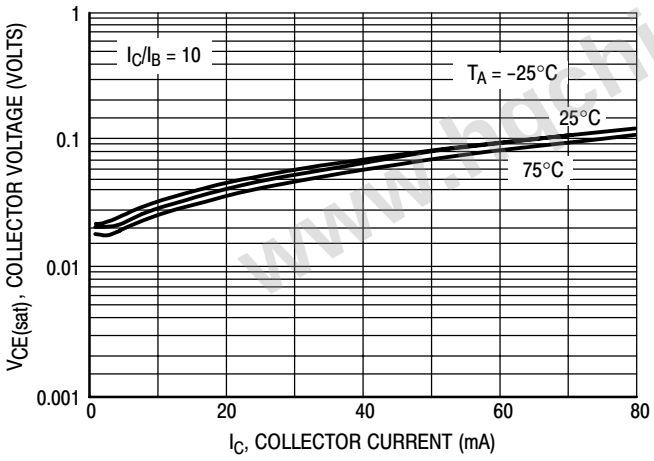


Figure 17. $V_{CE(sat)}$ versus I_C

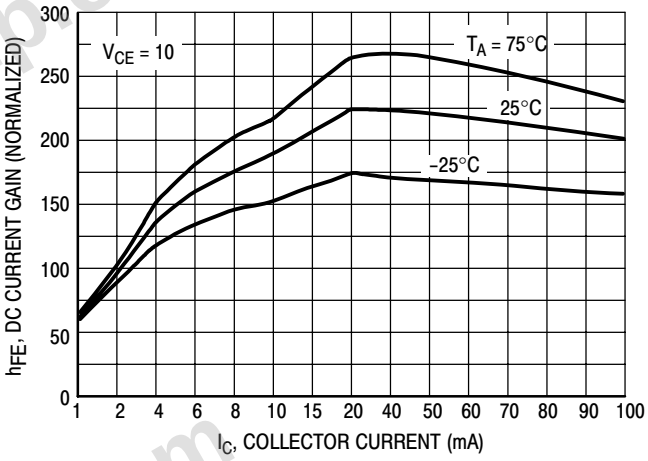


Figure 18. DC Current Gain

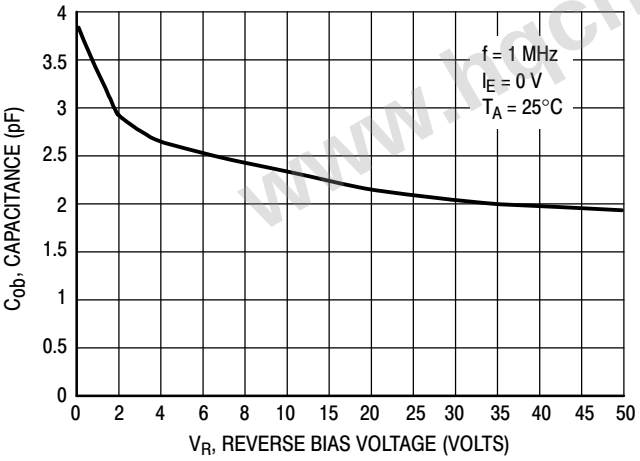


Figure 19. Output Capacitance

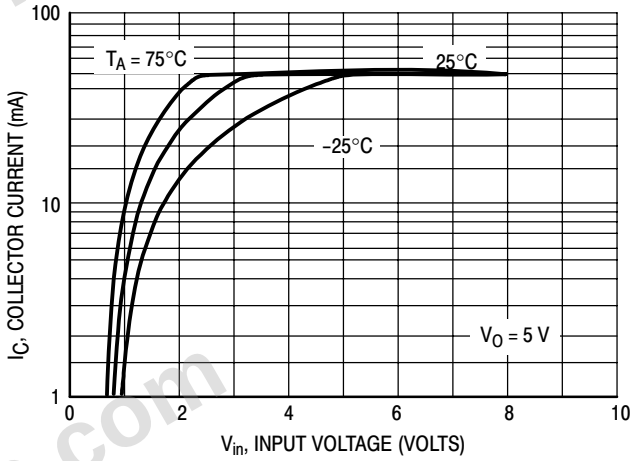


Figure 20. Output Current versus Input Voltage

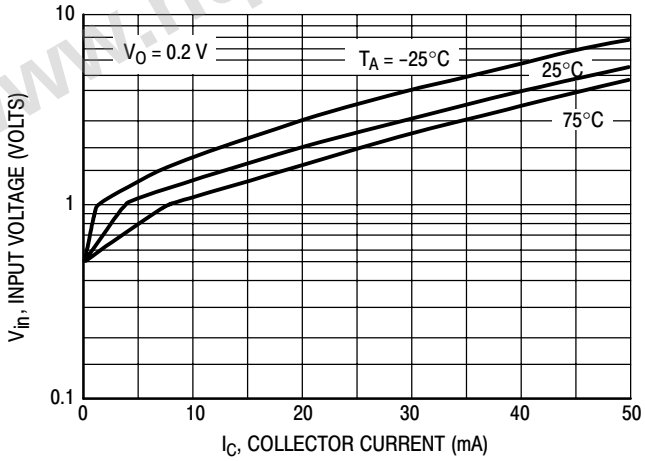


Figure 21. Input Voltage versus Output Current

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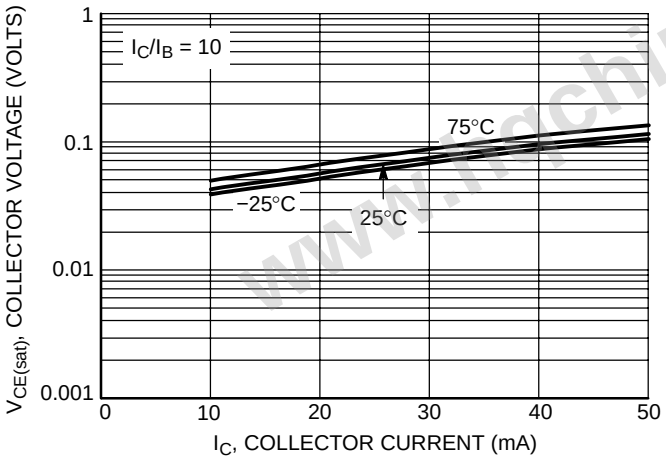


Figure 22. $V_{CE(sat)}$ versus I_C

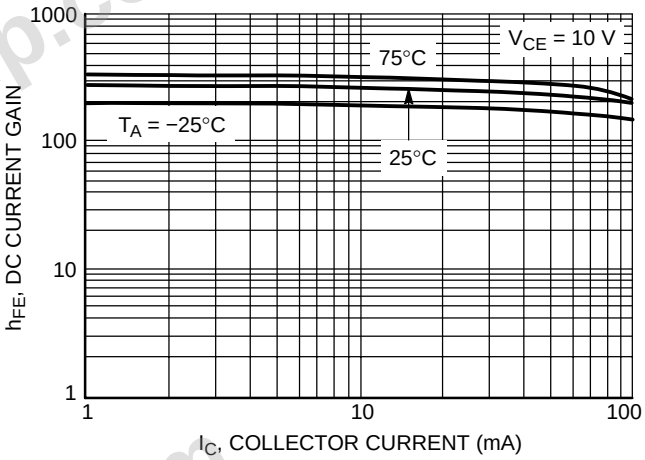


Figure 23. DC Current Gain

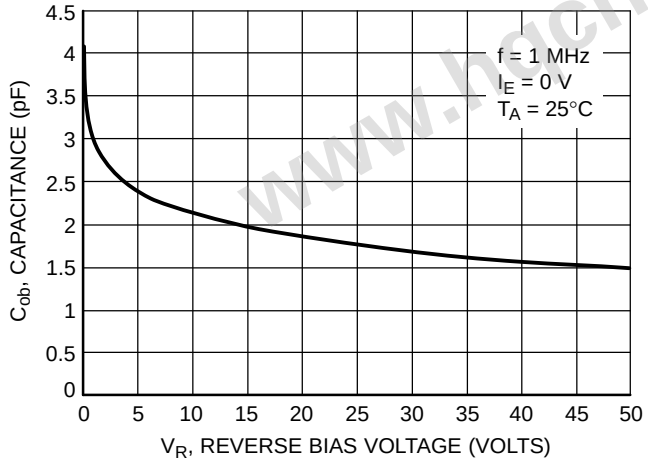


Figure 24. Output Capacitance

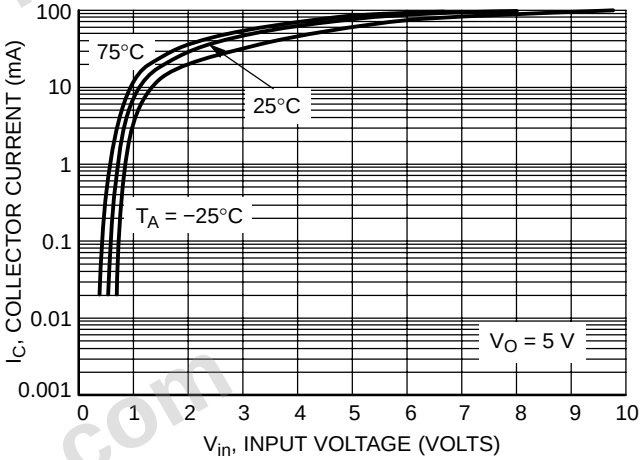


Figure 25. Output Current versus Input Voltage

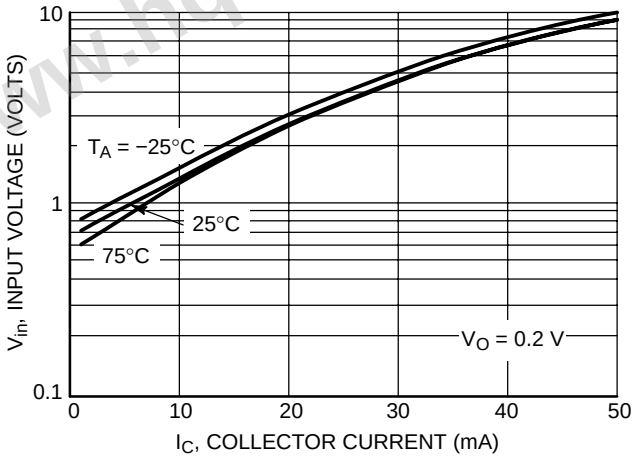


Figure 26. Input Voltage versus Output Current

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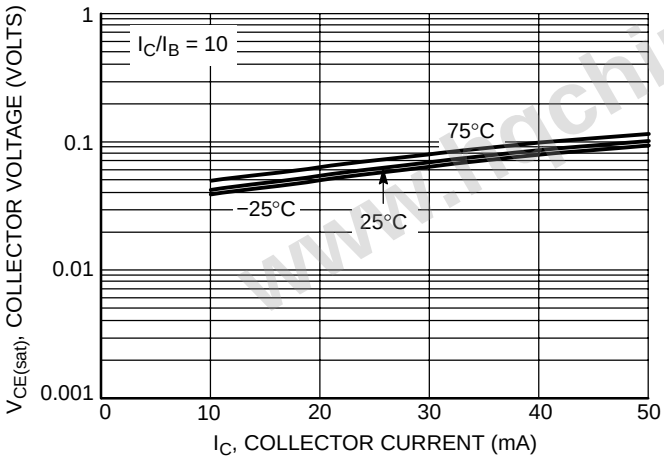


Figure 27. $V_{CE(sat)}$ versus I_C

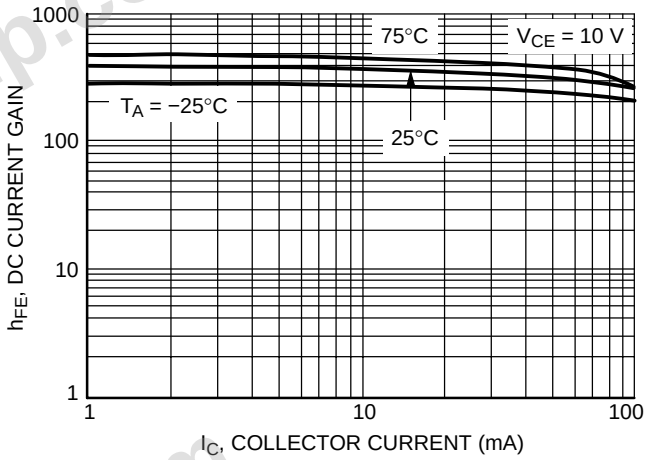


Figure 28. DC Current Gain

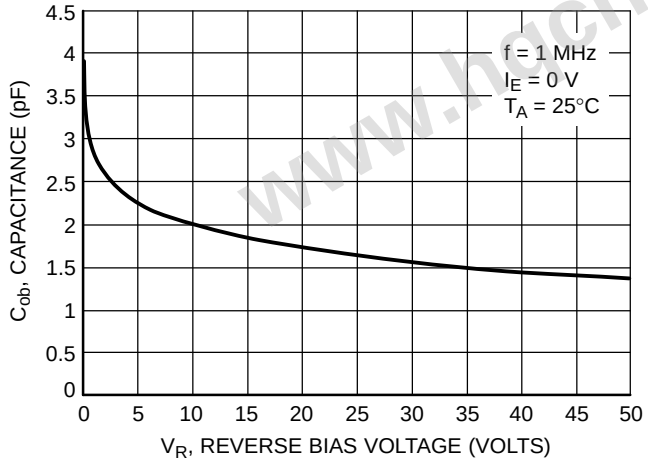


Figure 29. Output Capacitance

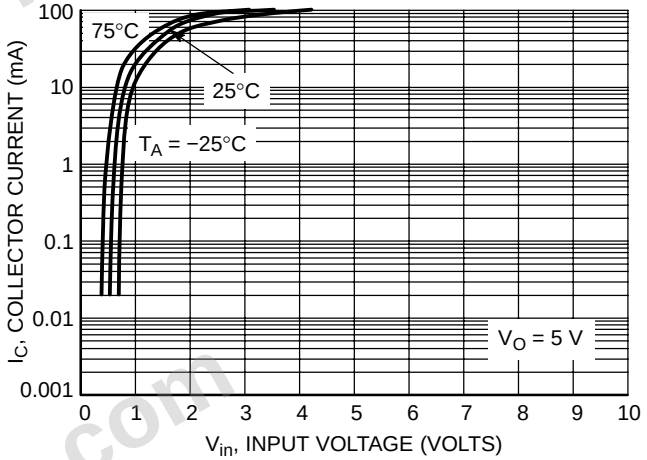


Figure 30. Output Current versus Input Voltage

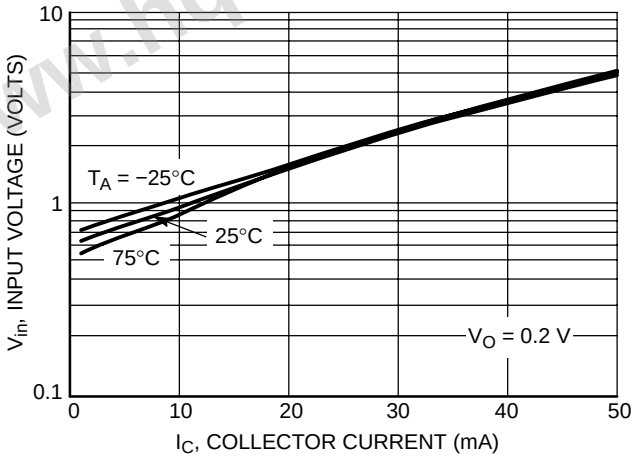


Figure 31. Input Voltage versus Output Current

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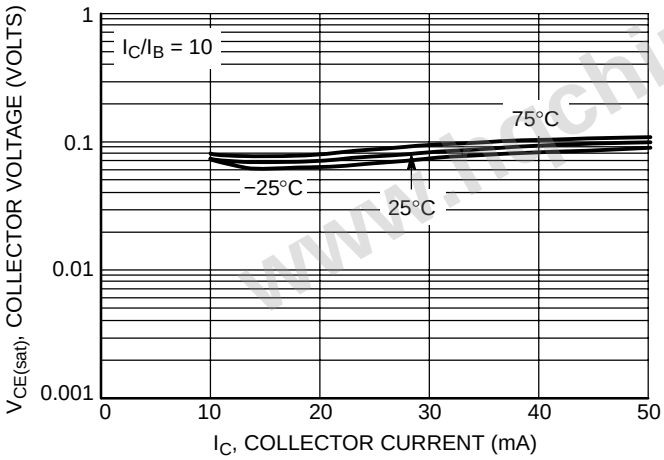


Figure 32. $V_{CE(sat)}$ versus I_C

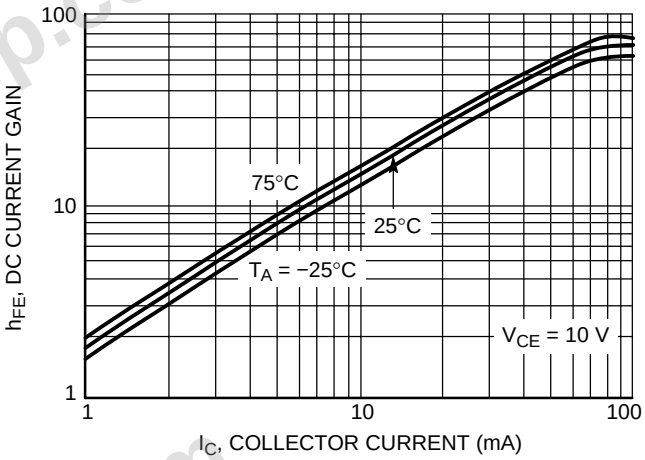


Figure 33. DC Current Gain

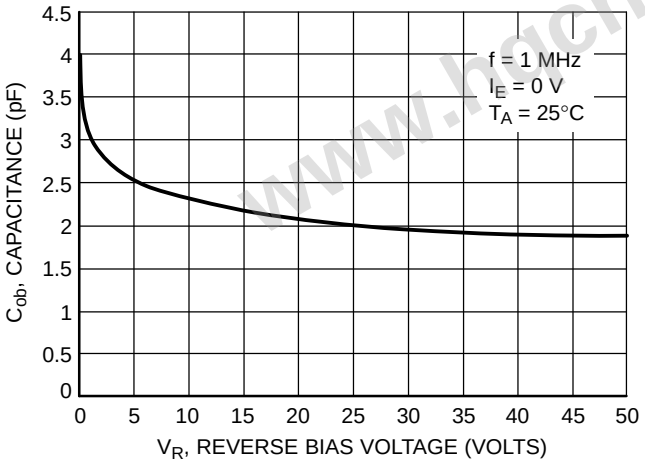


Figure 34. Output Capacitance

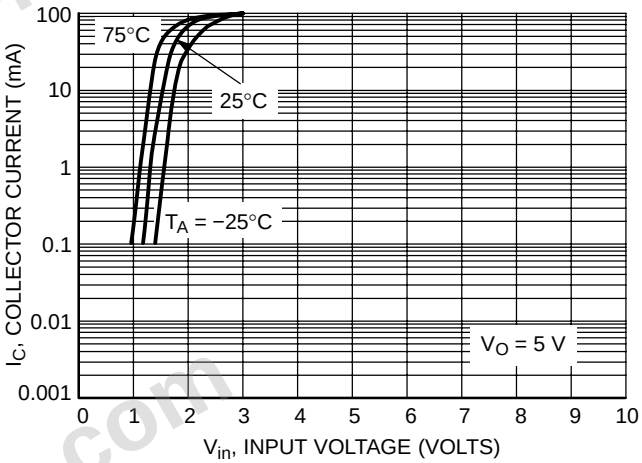


Figure 35. Output Current versus Input Voltage

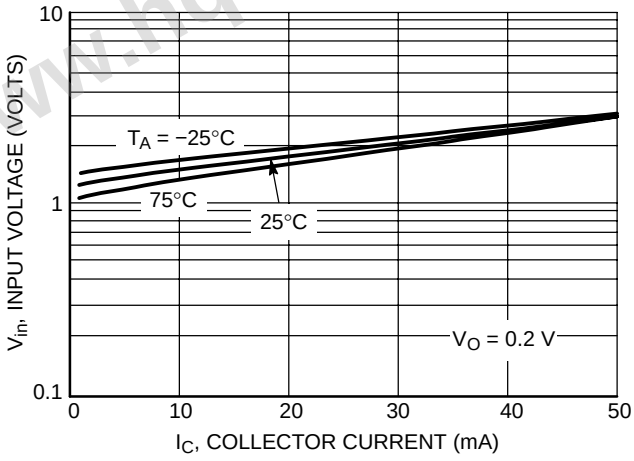


Figure 36. Input Voltage versus Output Current

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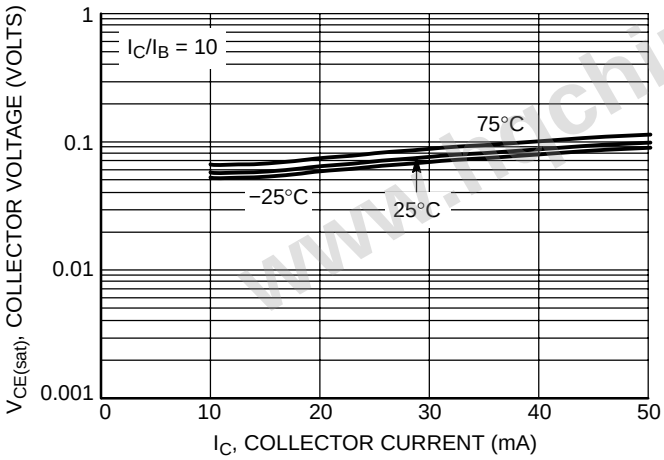


Figure 37. $V_{CE(sat)}$ versus I_C

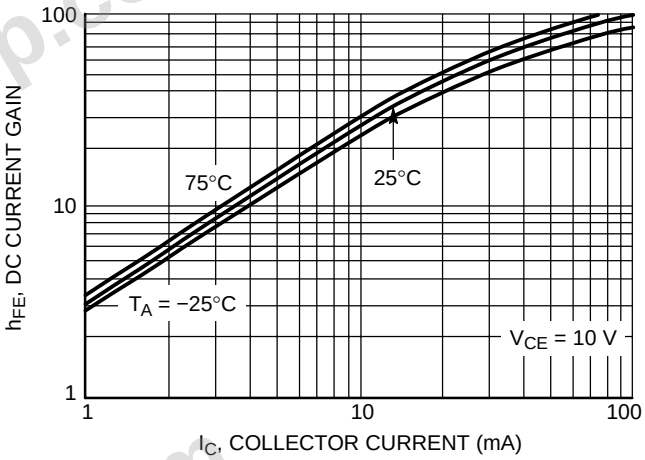


Figure 38. DC Current Gain

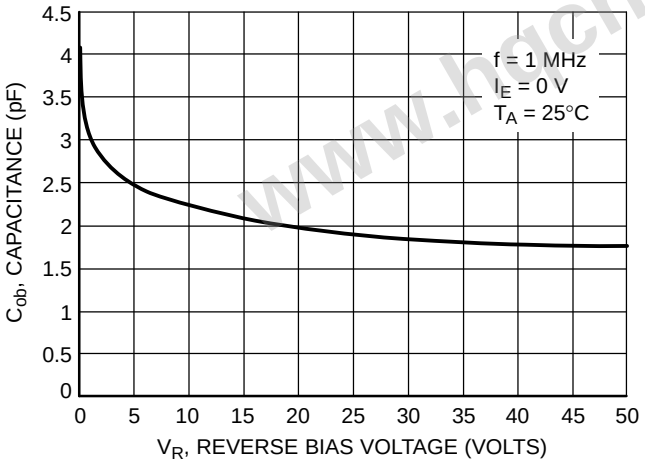


Figure 39. Output Capacitance

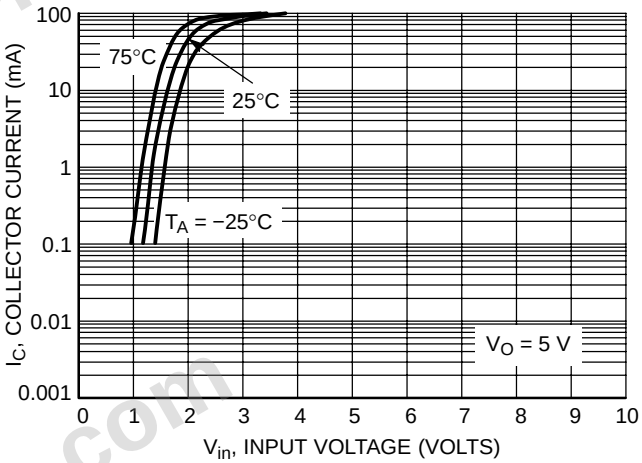


Figure 40. Output Current versus Input Voltage

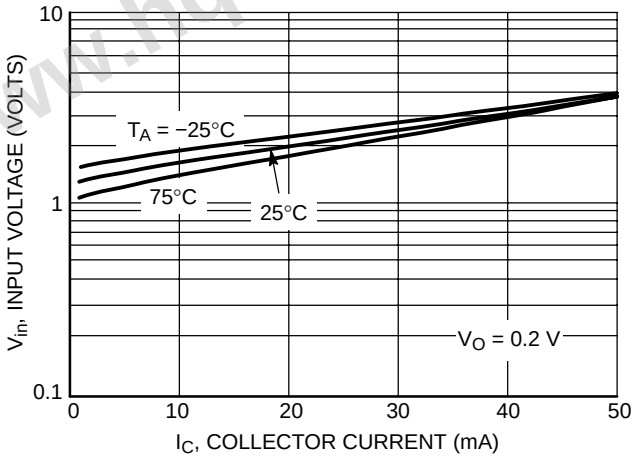


Figure 41. Input Voltage versus Output Current

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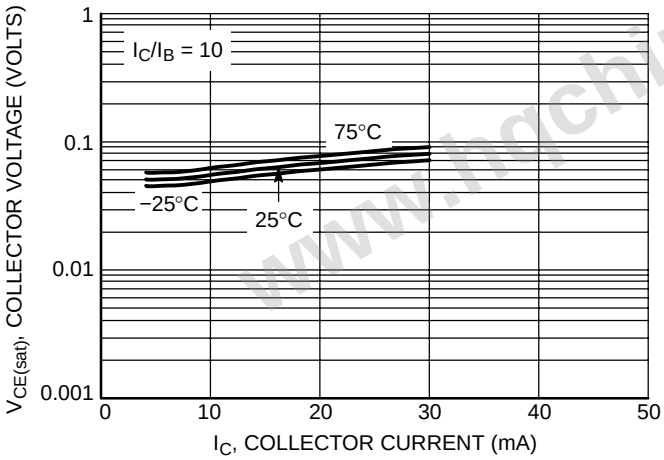


Figure 42. $V_{CE(sat)}$ versus I_C

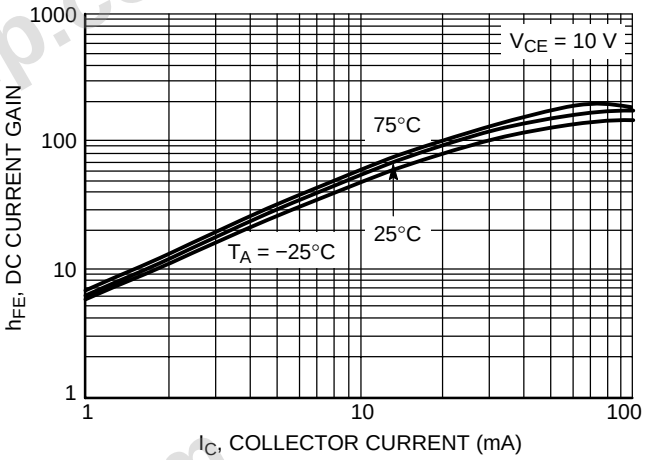


Figure 43. DC Current Gain

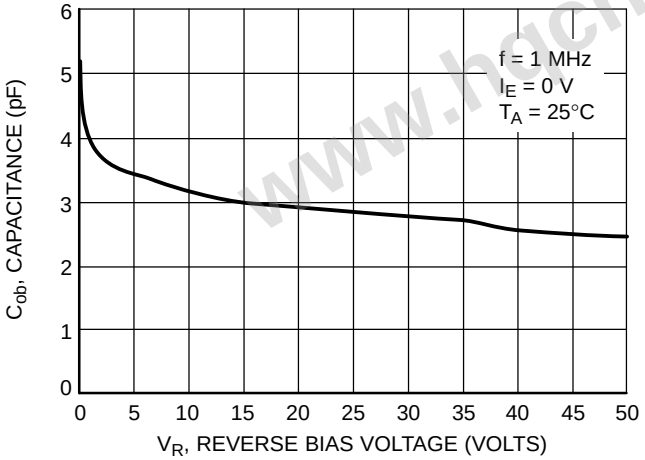


Figure 44. Output Capacitance

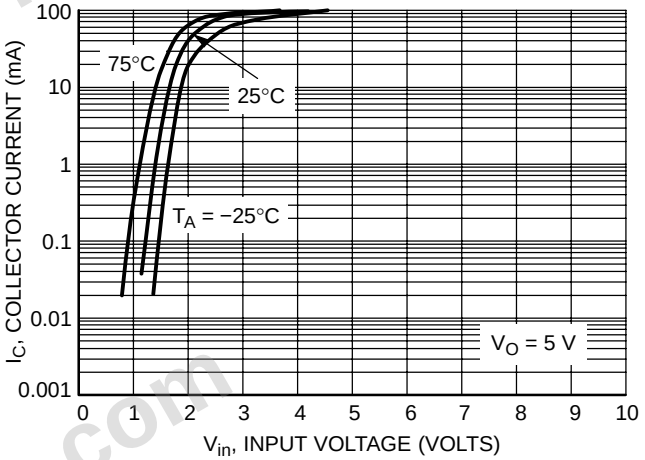


Figure 45. Output Current versus Input Voltage

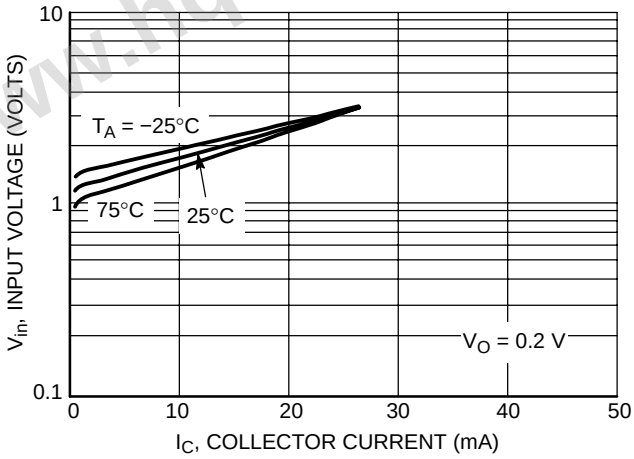


Figure 46. Input Voltage versus Output Current

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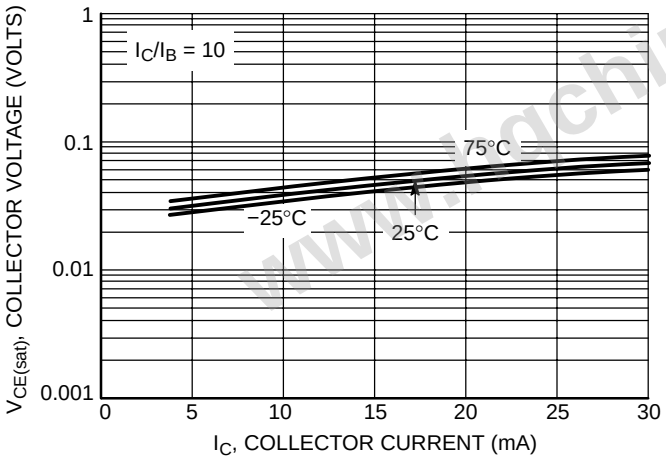


Figure 47. $V_{CE(sat)}$ versus I_C

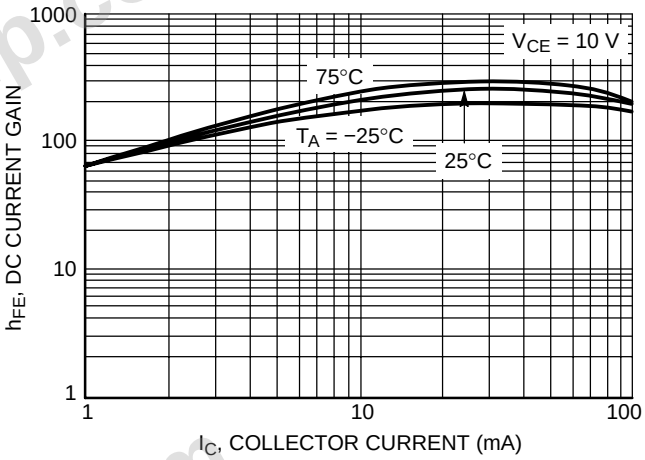


Figure 48. DC Current Gain

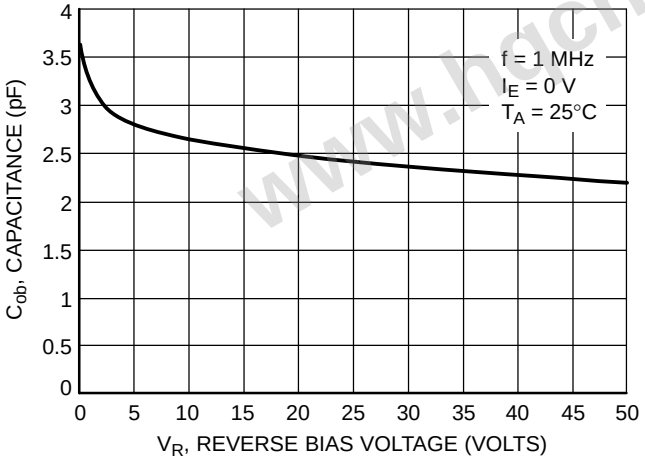


Figure 49. Output Capacitance

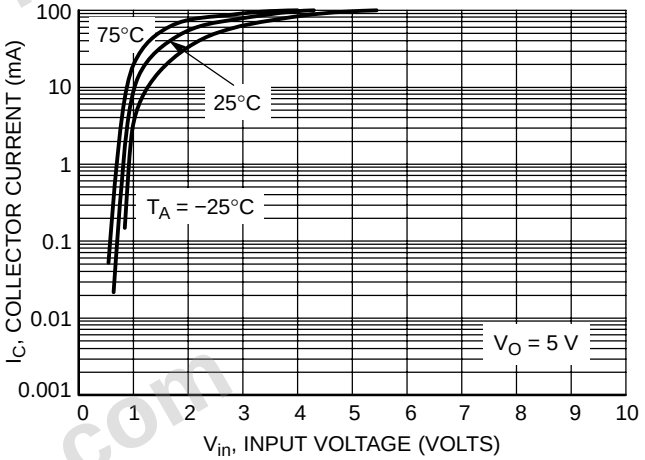


Figure 50. Output Current versus Input Voltage

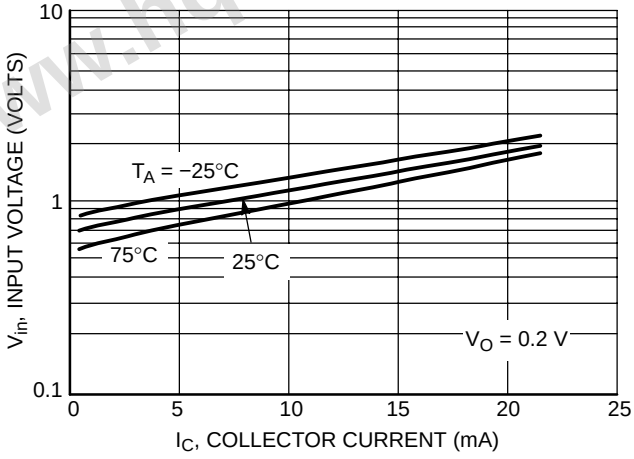


Figure 51. Input Voltage versus Output Current

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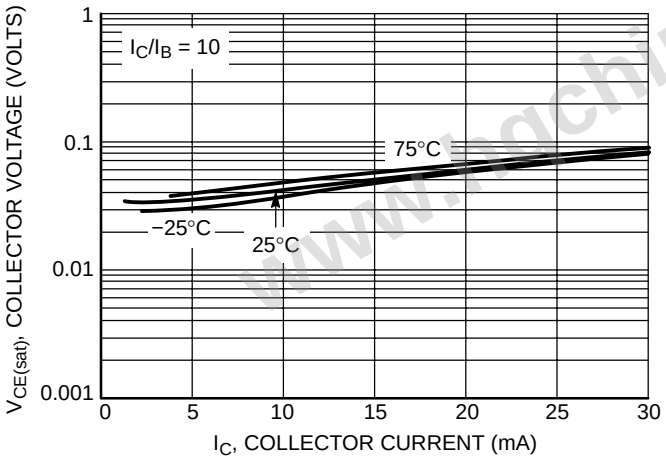


Figure 52. $V_{CE(sat)}$ versus I_C

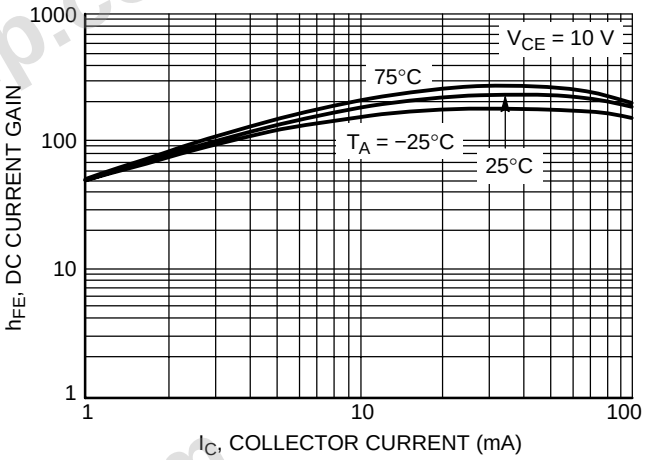


Figure 53. DC Current Gain

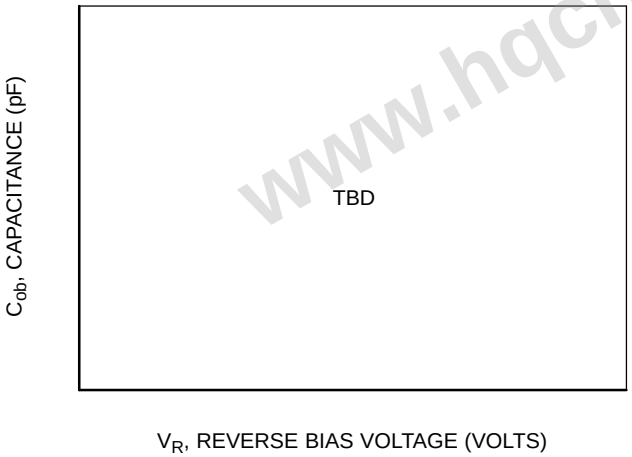


Figure 54. Output Capacitance

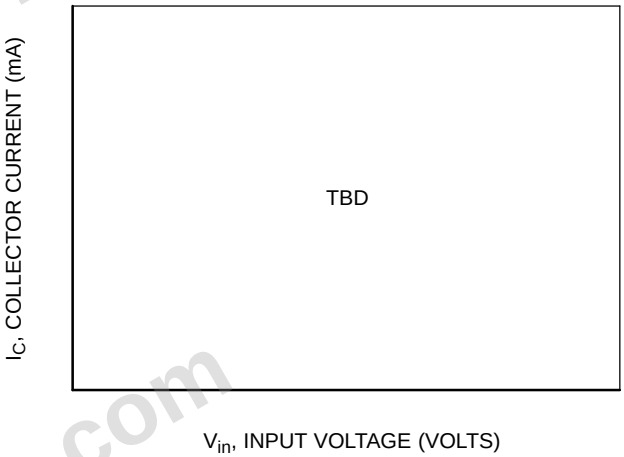


Figure 55. Output Current versus Input Voltage

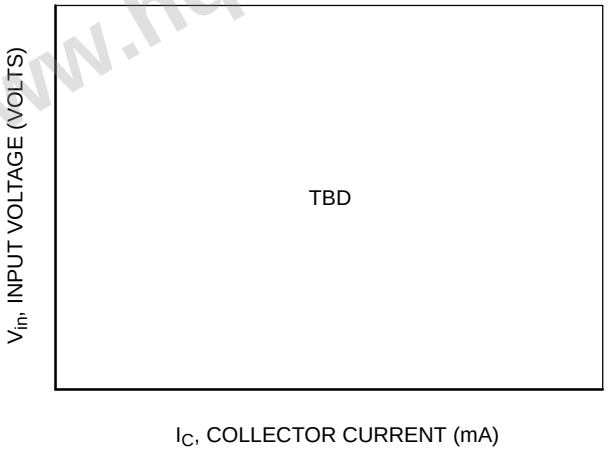


Figure 56. Input Voltage versus Output Current

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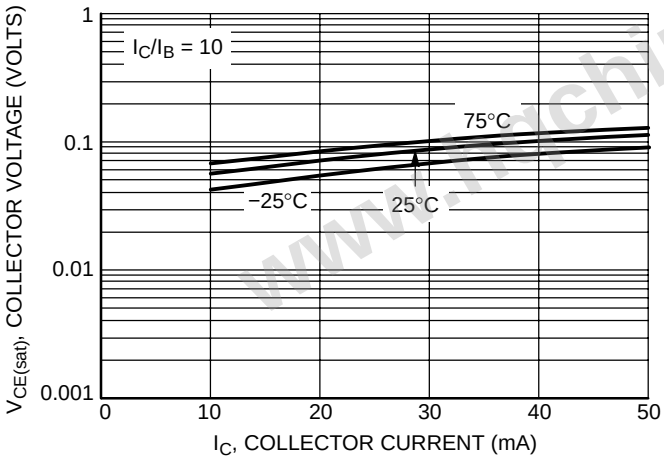


Figure 57. $V_{CE(sat)}$ versus I_C

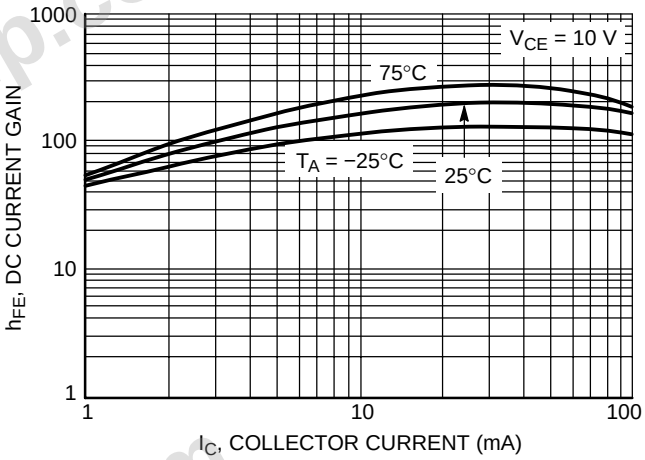


Figure 58. DC Current Gain

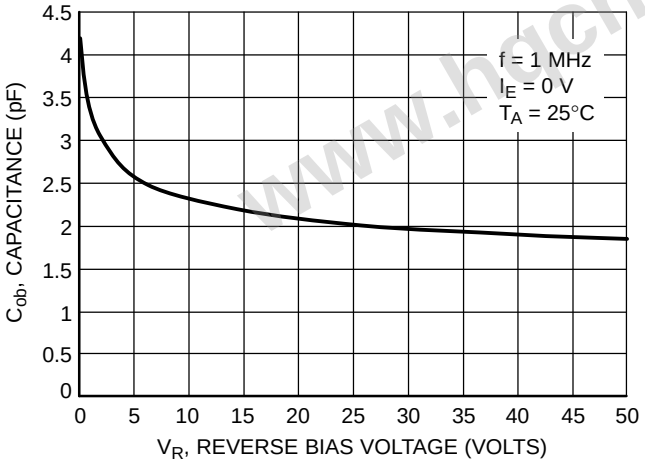


Figure 59. Output Capacitance

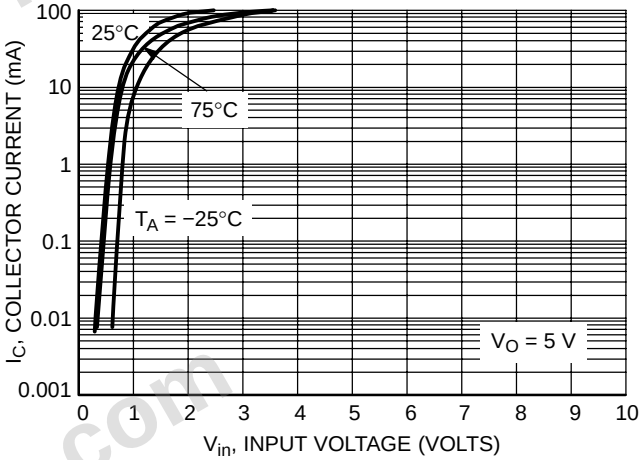


Figure 60. Output Current versus Input Voltage

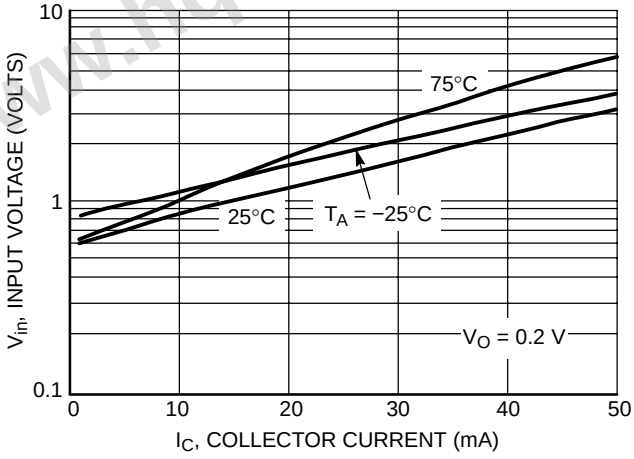


Figure 61. Input Voltage versus Output Current

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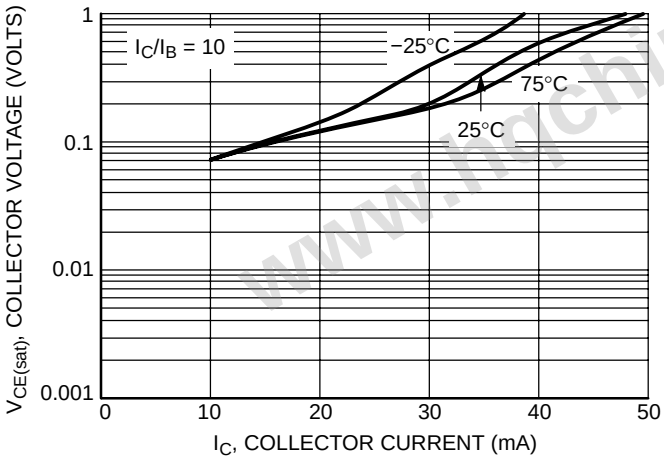


Figure 62. $V_{CE(sat)}$ versus I_C

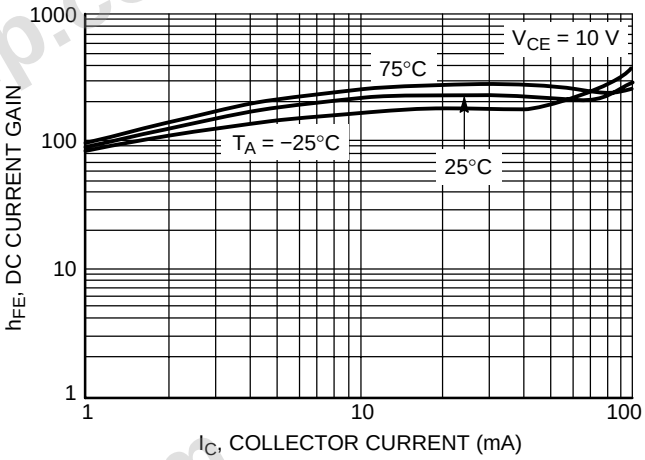


Figure 63. DC Current Gain

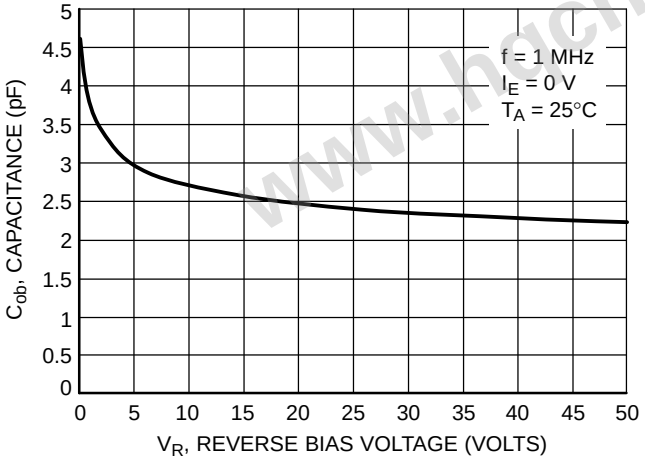


Figure 64. Output Capacitance

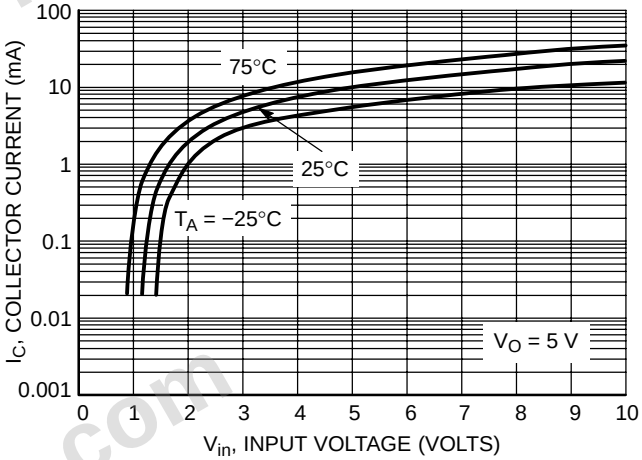


Figure 65. Output Current versus Input Voltage

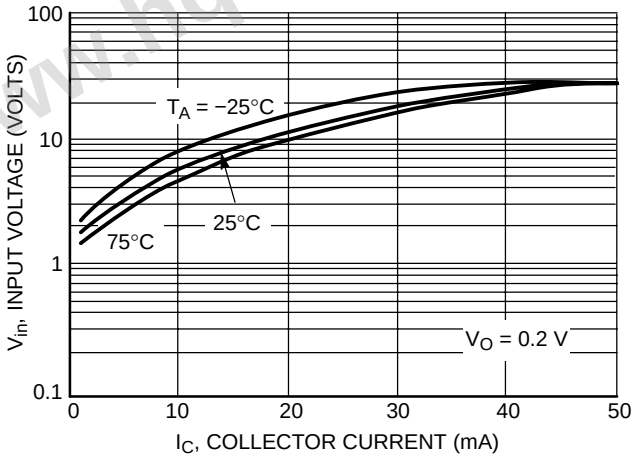


Figure 66. Input Voltage versus Output Current

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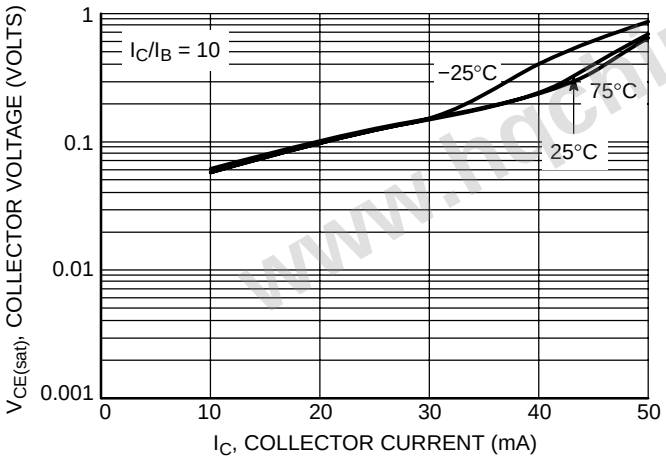


Figure 67. $V_{CE(sat)}$ versus I_C

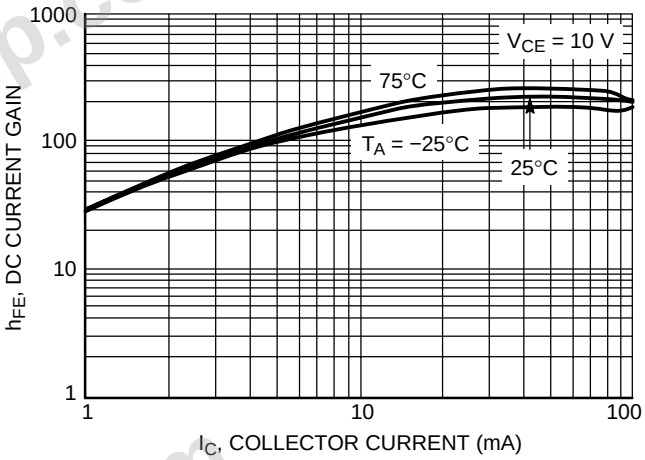


Figure 68. DC Current Gain

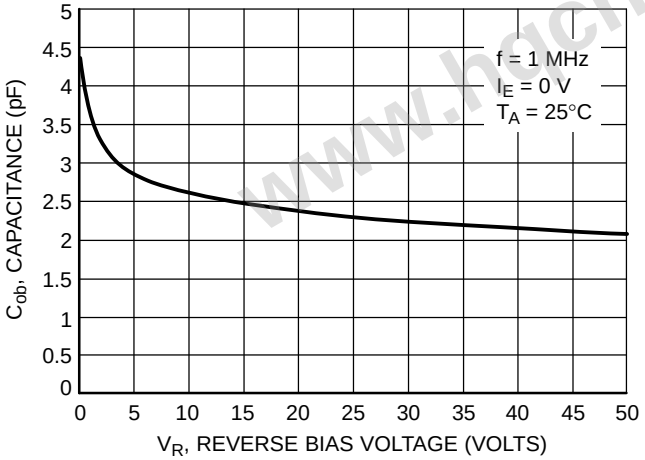


Figure 69. Output Capacitance

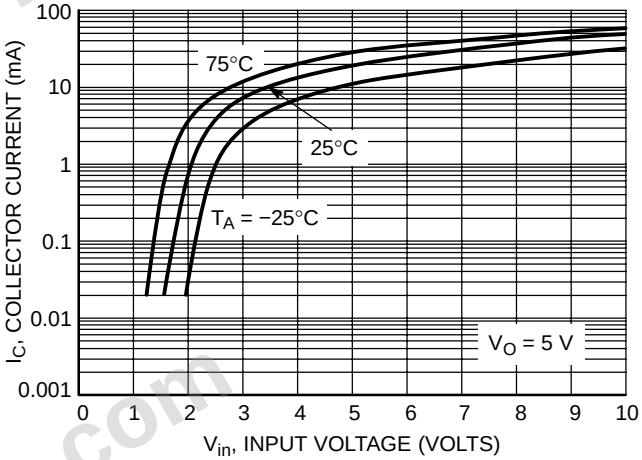


Figure 70. Output Current versus Input Voltage

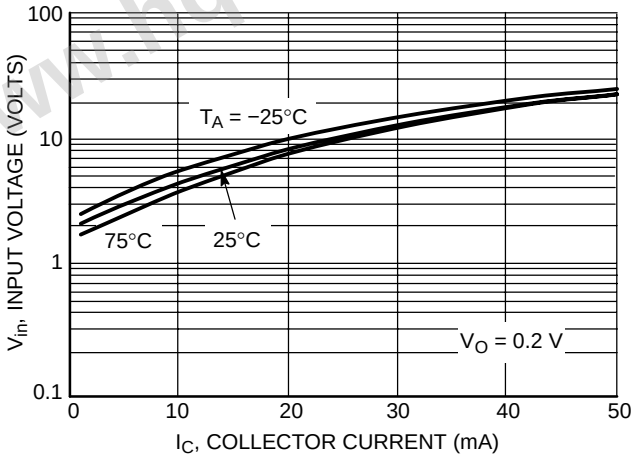
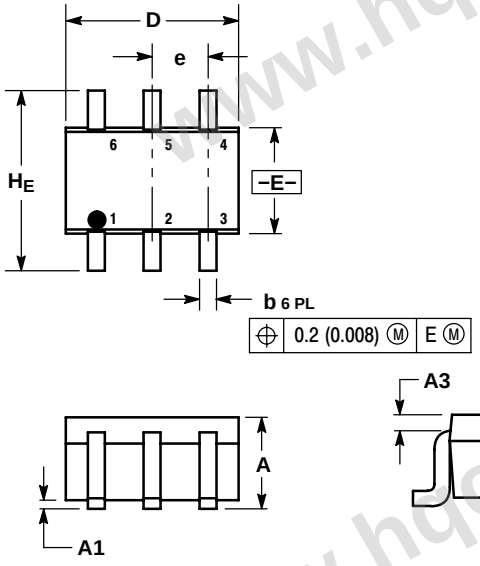


Figure 71. Input Voltage versus Output Current

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PACKAGE DIMENSIONS

SC−88 (SOT−363)
CASE 419B−02
ISSUE V

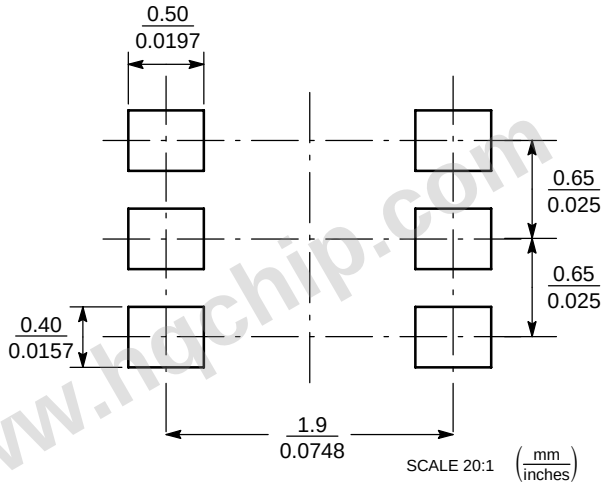


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. 419B−01 OBSOLETE, NEW STANDARD 419B−02.

	MILLIMETERS			INCHES		
DIM	MIN	NOM	MAX	MIN	NOM	MAX
A	0.80	0.95	1.10	0.031	0.037	0.043
A1	0.00	0.05	0.10	0.000	0.002	0.004
A3	0.20 REF			0.008 REF		
b	0.10	0.21	0.30	0.004	0.008	0.012
C	0.10	0.14	0.25	0.004	0.005	0.010
D	1.80	2.00	2.20	0.070	0.078	0.086
E	1.15	1.25	1.35	0.045	0.049	0.053
e	0.65 BSC			0.026 BSC		
L	0.10	0.20	0.30	0.004	0.008	0.012
H_E	2.00	2.10	2.20	0.078	0.082	0.086

STYLE 1:
PIN 1. EMITTER 2
2. BASE 2
3. COLLECTOR 1
4. EMITTER 1
5. BASE 1
6. COLLECTOR 2

SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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