# MP5035

## 2.9V to 22V, 50mA to 2A, Configurable Current Limit Switch in TSOT23-6 Package

## DESCRIPTION

The MP5035 is a protection device designed to protect circuitry on the output from transients on the input. It also protects the input from shorts and transients on the output.

During start-up, the inrush current is limited by the slew rate at the output. The slew rate is controlled by the DV/DT pin.

The output load maximum is current-limited. The current-limit value is controlled by an external resistor connected from the ILIMIT pin to GND. When ILIMIT is floating, the current limit is fixed at 300mA.

The MP5035 is available in a TSOT23-6 package.

## FEATURES

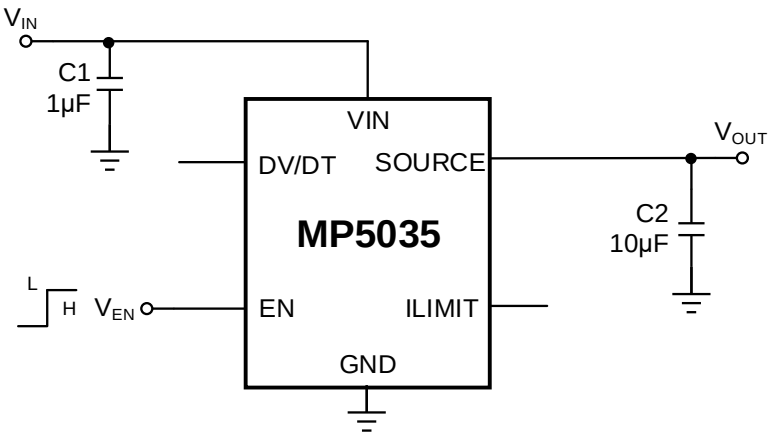
- Wide 2.9V to 22V Operating Input Voltage ($V_{IN}$) Range
- 26V Absolute Maximum Transient $V_{IN}$
- Integrated 82mΩ Power MOSFET
- Adjustable Current Limit or Fixed Current Limit when Floating the ILIMIT Pin
- Soft-Start Time Configurable through the DV/DT Pin
- Fast Response for Hard Short Protection
- Over-Current Protection (OCP) with Hiccup Mode
- Thermal Shutdown and Automatic Retry
- Available in a TSOT23-6 Package

## APPLICATIONS

- Hot Swaps
- Power Meters
- IP Cameras
- USB Power Distribution
- USB Protection
- USB3.1 Power Delivery

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## TYPICAL APPLICATION





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## ORDERING INFORMATION

| Part Number* | Package | Top Marking | MSL Rating |
|---|---|---|---|
| MP5035GJ | TSOT23-6 | *See Below* | 1 |

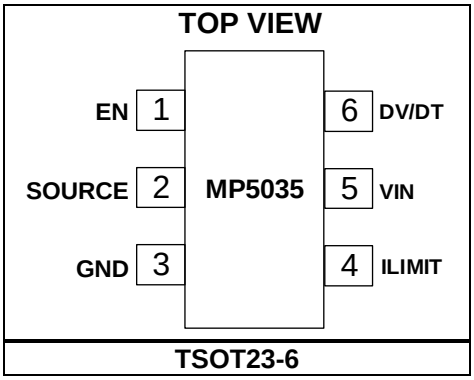
* For Tape & Reel, add suffix -Z (e.g. MP5035GJ-Z).

## TOP MARKING

BNEY

BNE: Product code of MP5035GJ
Y: Year code

## PACKAGE REFERENCE





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## PIN FUNCTIONS

| Pin # | Name | Description |
|---|---|---|
| 1 | EN | **Enable.** Pull the EN pin high to enable the MP5035. Float EN or pull EN to GND to disable the MP5035. For quick start-up, pull EN up to VIN through a 300kΩ resistor. |
| 2 | SOURCE | **Source of the internal power MOSFET and output terminal of the IC.** |
| 3 | GND | **System ground.** |
| 4 | ILIMIT | **Current limit setting.** Place a resistor between ILIMIT and ground to set the current limit value. Float ILIMIT for a fixed 300mA current limit. |
| 5 | VIN | **Supply voltage.** The MP5035 operates from a 2.9V to 22V input rail. A ceramic capacitor is required to decouple the input rail. Connect VIN using a wide PCB trace. |
| 6 | DV/DT | **DV/DT.** Connect a capacitor from DV/DT to ground to set the DV/DT slew rate. |

## ABSOLUTE MAXIMUM RATINGS (1)

VIN, SOURCE ..... -0.3V to +26V
All other pins .....-0.3V to +5.5V
Junction temperature ..... -40°C to +150°C
Lead temperature .....260°C
Continuous power dissipation ($T_A$ = 25°C) (2) (4)
TSOT23-6 ..... 1.89W

### *ESD Ratings*

Human body model (HBM)…….. ±2000V
Charged device model (CDM) ..... ±750V

### *Recommended Operating Conditions* (3)

Supply voltage ($V_{IN}$) ..... 2.9V to 22V
Operating junction temp ($T_J$) .... -40°C to +125°C

### *Thermal Resistance* $\theta_{JA}$ $\theta_{JC}$

***TSOT23-6***

EV5035-J-00A (4).....66.....23..... °C/W
JESD51-7 (5).....100…...55…... °C/W

**Notes:**

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature, $T_J$ (MAX), the junction-to-ambient thermal resistance, $\theta_{JA}$, and the ambient temperature, $T_A$. The maximum allowable continuous power dissipation on EV5035-J-00A board at any ambient temperature is calculated by $P_D$ (MAX) = ($T_J$ (MAX) - $T_A$) / $\theta_{JA}$. Exceeding the maximum allowable power dissipation can cause excessive die temperature, and the MP5035 may go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on EV5035-J-00A, 2-layer PCB, 50mmx50mm.
5) The value of $\theta_{JA}$ given in this table is only valid for comparison with other packages and cannot be used for design purposes. These values were calculated in accordance with JESD51-7, and simulated on a specified JEDEC board. They do not represent the performance obtained in an actual application.


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## ELECTRICAL CHARACTERISTICS

**$V_{IN}$ = 12V, $R_{LIMIT}$ = NS, $C_{OUT}$ = 10µF, $T_J$ = -40°C to +125°C (6), typical value is tested at $T_J$ = 25°C, unless otherwise noted.**

| Parameter | Symbol | Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **Supply Current** | | | | | | |
| Quiescent supply current | $I_Q$ | EN = high | | 550 | | µA |
| Shutdown supply current | $I_S$ | EN = GND | | 17 | | µA |
| **Power FET** | | | | | | |
| On resistance | $R_{DS(ON)}$ | $I_{OUT}$ = 1A | | 82 | | mΩ |
| Turn-on delay | $t_{DELAY}$ | From EN rising to $V_{OUT}$ rising, DV/DT floating | | 2.5 | | ms |
| Off-state leakage current | $I_{OFF}$ | EN = 0V | | 0.1 | 1 | µA |
| **Under-Voltage Protection** | | | | | | |
| Under-voltage lockout rising threshold | $V_{UVLO}$ | | 2.55 | 2.7 | 2.85 | V |
| UVLO hysteresis | $V_{UVLOHYS}$ | | | 200 | | mV |
| **DV/DT** | | | | | | |
| DV/DT slew rate | dV/dt | DV/DT floating, $T_J$ = -40°C to +125°C | 1.3 | 2 | 2.7 | V/ms |
| DV/DT current | $I_{DV/DT}$ | $V_{DV/DT}$ = 0.5V $T_J$ = -40°C to +125°C | 4.5 | 6.5 | 8.5 | µA |
| **Current Limit** | | | | | | |
| Current limit during normal operation | $I_{LIMIT_NO}$ | Float the ILIMIT pin, $T_J$ = 25°C | 0.28 | 0.3 | 0.32 | A |
| | | $R_{LIMIT}$ = 549Ω, $T_J$ = 25°C | 1.85 | 2 | 2.15 | A |
| | | $R_{LIMIT}$ = 1.5kΩ, $T_J$ = 25°C | 0.7 | 0.75 | 0.8 | A |
| | | $R_{LIMIT}$ = 5.6kΩ, $T_J$ = 25°C | 0.185 | 0.2 | 0.215 | A |
| **Enable** | | | | | | |
| Enable rising threshold | $V_{EN_RISING}$ | | 1.86 | 2 | 2.16 | V |
| Enable hysteresis | $V_{EN_HYS}$ | | | 350 | | mV |
| Enable pull-down resistor | $R_{EN_DOWN}$ | | | 2.2 | | MΩ |
| **Output Discharge** | | | | | | |
| Discharge resistance | $R_{DIS}$ | $V_{IN}$ = 5V | | 540 | | Ω |
| **Over-Temperature Protection** | | | | | | |
| Thermal shutdown (7) | $T_{SD}$ | | | 175 | | °C |
| Thermal hysteresis (7) | $T_{SD_HYS}$ | | | 50 | | °C |

**Notes:**

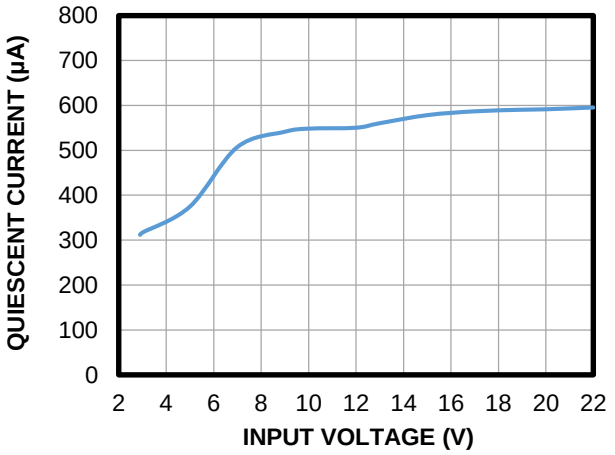
6) Guaranteed by over-temperature correlation.
7) Guaranteed by engineering sample characterization.


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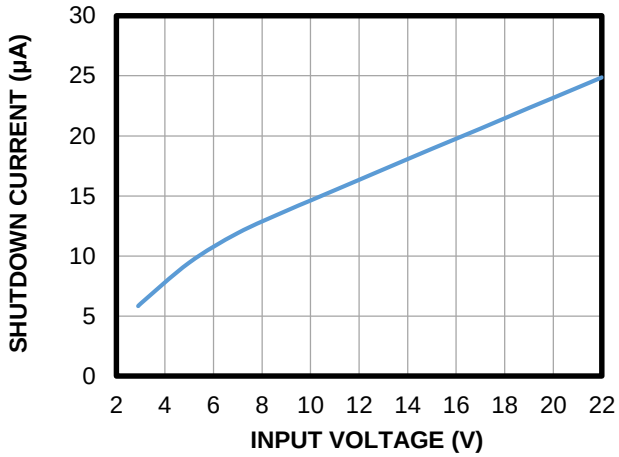
## TYPICAL PERFORMANCE CHARACTERISTICS

**$V_{IN}$ = 12V, $V_{EN}$ = 5V, $R_{LIMIT}$ = 549Ω, $C_{OUT}$ = 10µF, $T_A$ = 25°C, unless otherwise noted.**

### Quiescent Current vs. Input Voltage

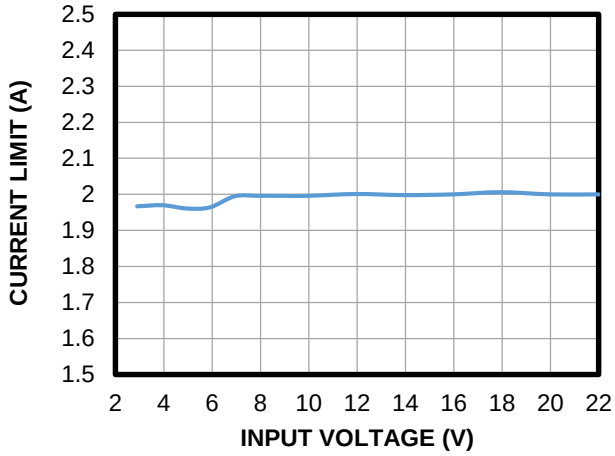



### Shutdown Current vs. Input Voltage



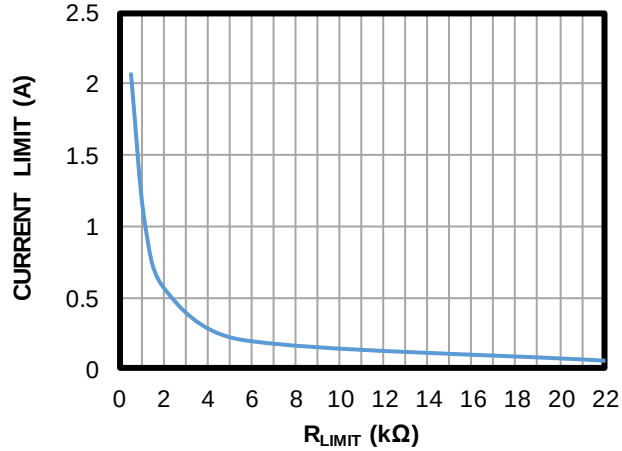

### Current Limit vs. Input Voltage

$R_{LIMIT}$ = 549Ω

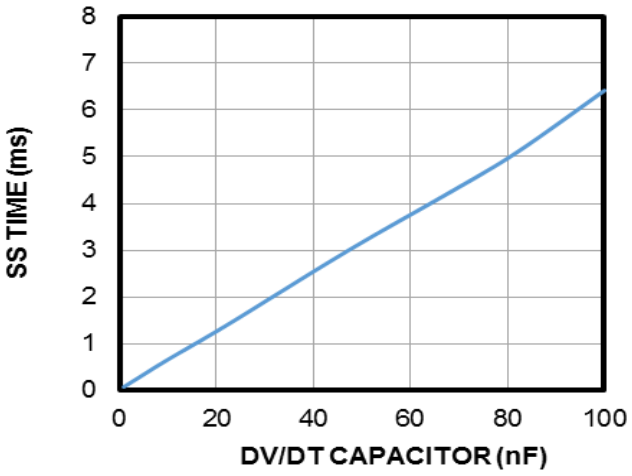



### Current Limit vs. Current Limit Resistor

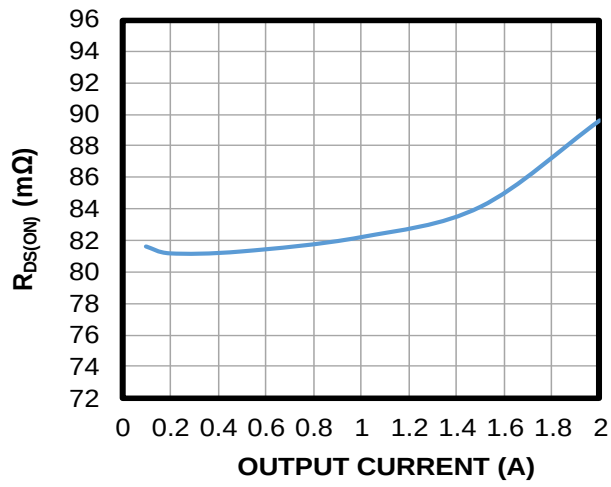
$R_{LIMIT}$ = 549Ω to 22kΩ




### SS Time vs. DV/DT Capacitor




### $R_{DS(ON)}$ vs. Output Current



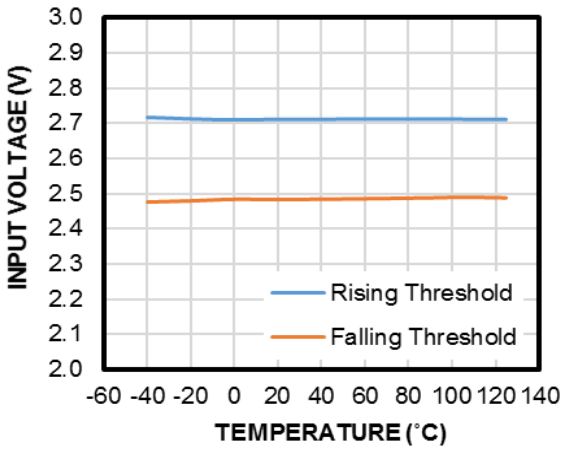


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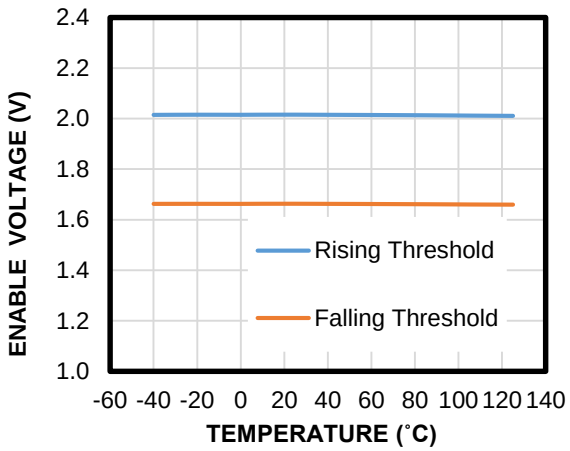
## TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

**$V_{IN}$ = 12V, $V_{EN}$ = 5V, $R_{LIMIT}$ = 549Ω, DV/DT floating, $C_{OUT}$ = 10µF, $T_A$ = 25°C, unless otherwise noted.**

**VIN UVLO Rising/Falling Threshold vs. Temperature**




**EN Rising/Falling Threshold vs. Temperature**



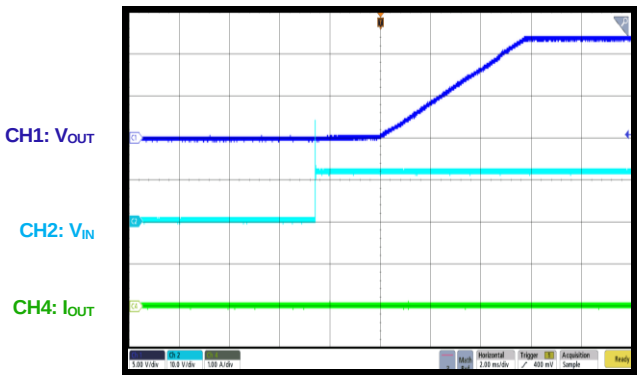


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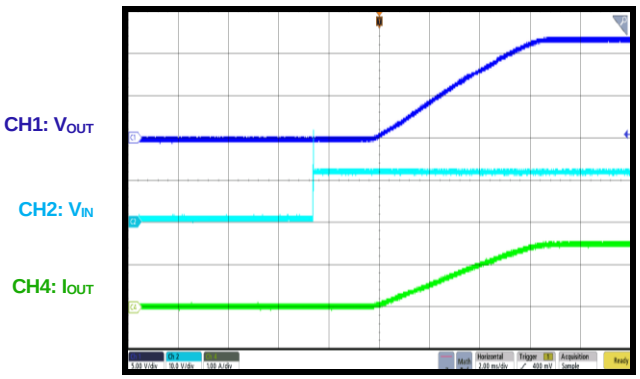
## TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

**$V_{IN}$ = 12V, $V_{EN}$ = 5V, $R_{LIMIT}$ = 549Ω, DV/DT floating, $C_{OUT}$ = 10µF, $T_A$ = 25°C, unless otherwise noted.**

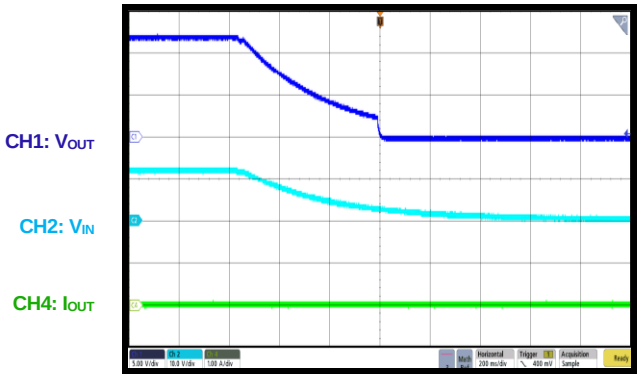
### Start-Up through VIN
$I_{OUT}$ = 0A



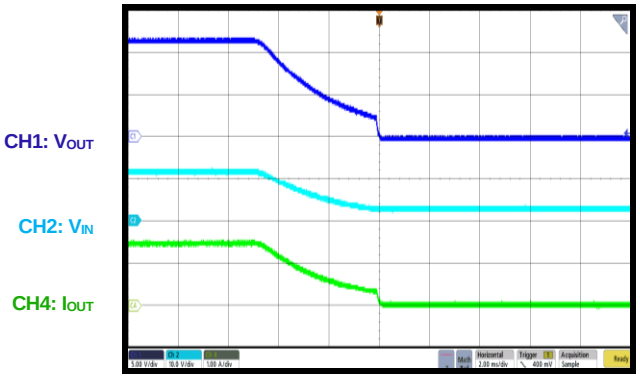

### Start-Up through VIN
$I_{OUT}$ = 1.5A



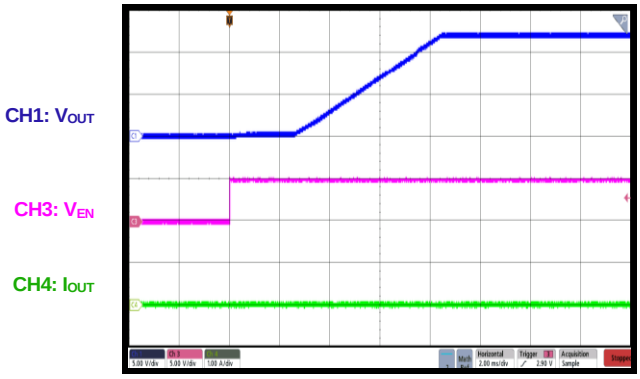

### Shutdown through VIN
$I_{OUT}$ = 0A



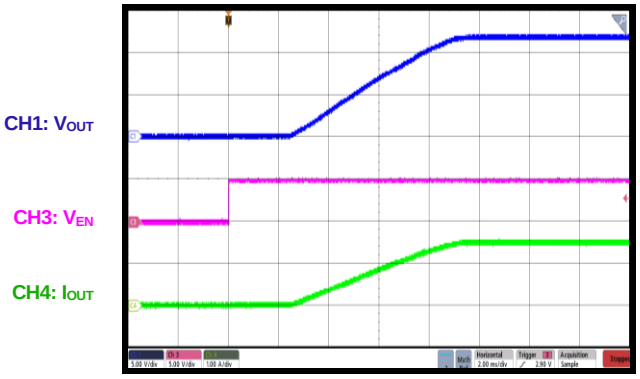

### Shutdown through VIN
$I_{OUT}$ = 1.5A




### Start-Up through EN
$I_{OUT}$ = 0A




### Start-Up through EN
$I_{OUT}$ = 1.5A





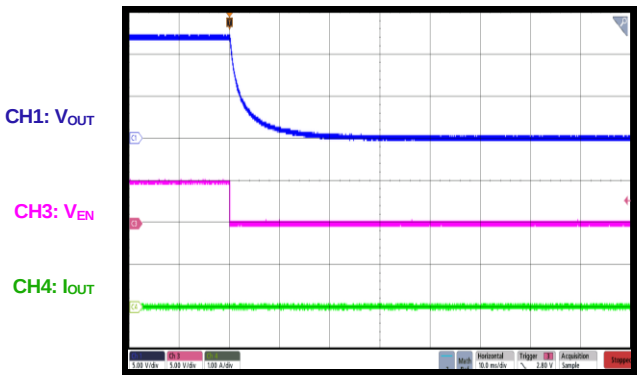
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## TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

**$V_{IN}$ = 12V, $V_{EN}$ = 5V, $R_{LIMIT}$ = 549Ω, DV/DT floating, $C_{OUT}$ = 10µF, $T_A$ = 25°C, unless otherwise noted.**

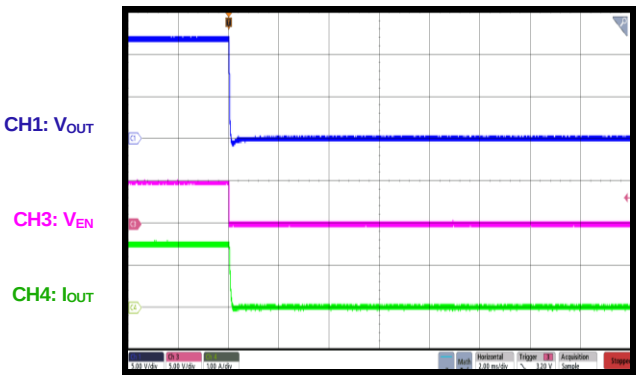
### Shutdown through EN

$I_{OUT}$ = 0A



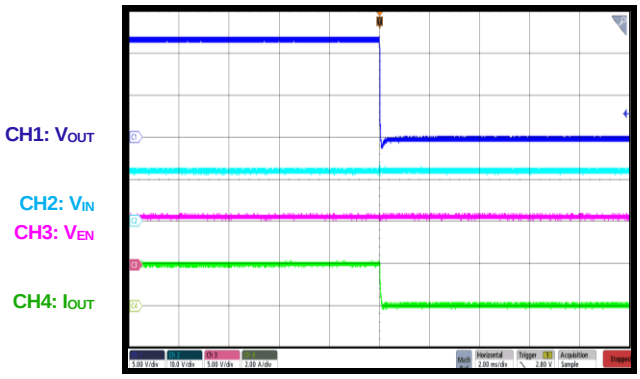

### Shutdown through EN

$I_{OUT}$ = 1.5A



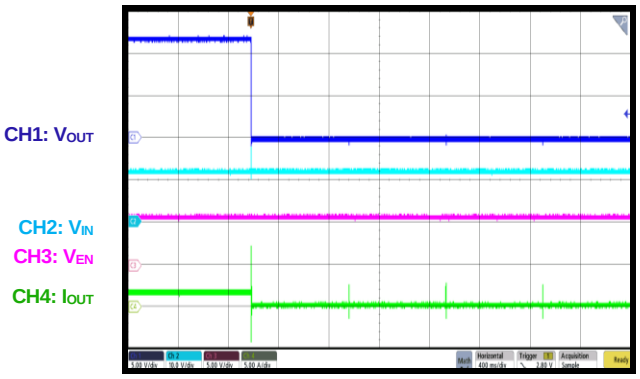

### Current Limit

Increase $I_{OUT}$ slowly



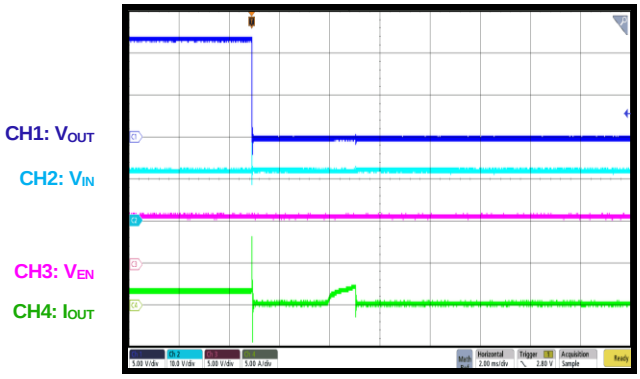

### Short Circuit during Normal Operation and Hiccup Mode

$I_{OUT}$ = 1.5A

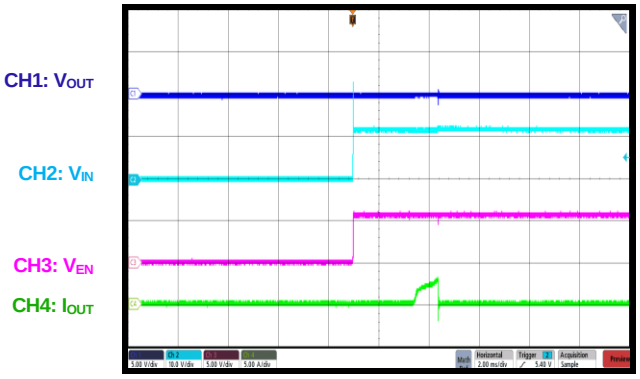



### Short Circuit Entry during Normal Operation

$I_{OUT}$ = 1.5A




### Short Circuit before Start-Up through VIN





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# FUNCTIONAL BLOCK DIAGRAM

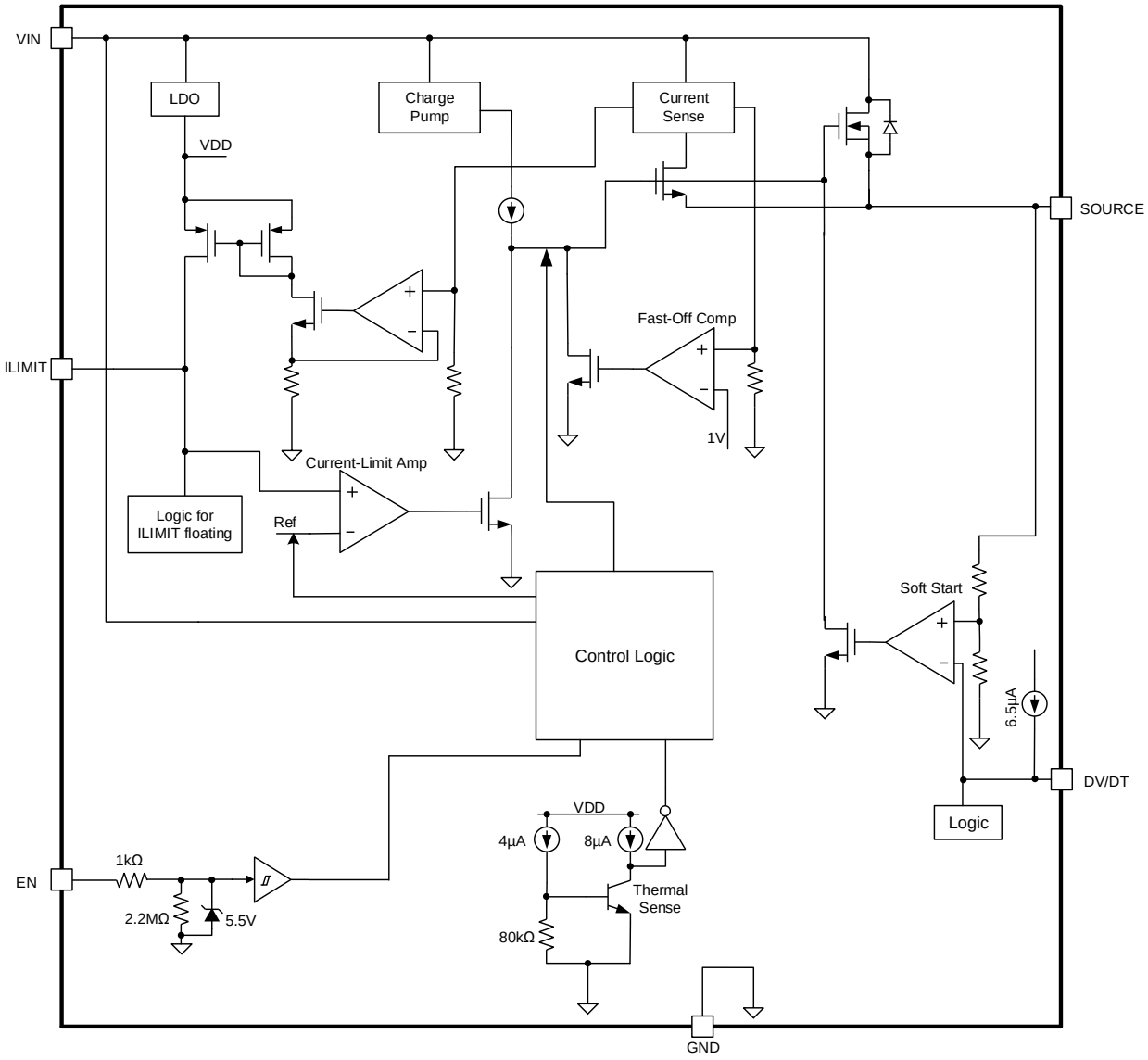



**Figure 1: Functional Block Diagram**


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## OPERATION

The MP5035 is designed to limit the inrush current to the load when a circuit card is inserted into a live backplane power source. This limits the backplane's voltage drop, as well as the dV/dt of the voltage to the load. The device offers an integrated solution to monitor the input voltage, output voltage, output current, and die temperature. This means that an external current-sense power resistor, power MOSFET, and thermal-sense device are not required.

### Under-Voltage Lockout (UVLO)

The MP5035 can be used in 2.9V to 22V input supply systems. There are high-energy transients during normal operation, or during hot swap. These transients depend on the parasitic inductance, wire resistance, and the capacitor at the VIN node. If a power clamp (TVS, Tranzorb) diode is not used, the e-fuse must be able to withstand this transient voltage. The MP5035 integrates a high-voltage MOSFET with up to 22V of continuous voltage and a maximum 26V transient input voltage. The device also uses a high-voltage circuit at the VIN node to guarantee safe operation.

### Soft Start (SS)

The soft-start time ($t_{SS}$) is related to the dV/dt slew rate and input voltage. $t_{SS}$ can be calculated with Equation (1):

$$t_{SS}(ms) = \frac{V_{IN}(V)}{dV/dt\ (V/ms)} \quad (1)$$

The dV/dt slew rate is controlled by the DV/DT pin. For more details, see the Setting the Soft-Start Time section on page 12.

### Current Limit

The MP5035 provides a constant current limit, which can be configured via an external resistor.

The current limit value is a function of the external current-limit resistor. $I_{LIMIT}$ can be calculated with Equation (2):

$$I_{LIMIT}(A) = \frac{0.58(V)}{R_{LIMIT}(\Omega)} \times 1940 \quad (2)$$

Where 1940 is the current-sense ratio.

Once the current limit threshold is reached, the internal circuit regulates the gate voltage to maintain a constant power MOSFET current. To limit the current, the gate to the source voltage must be regulated from 5V to about 1V. The typical response time is about 15µs. During this period, the output current may have a small overshoot.

If the current limit condition lasts longer than 2ms, the IC enters hiccup mode with 700ms of off time.

The MP5035 allows the ILIMIT pin to be floated during operation. If ILIMIT is floating, the current limit is set to 300mA internally.

When shorting ILIMIT to GND, the normal current limit is disabled, but the secondary current limit is functional. The secondary current limit is set to 8A internally. If the secondary current limit is triggered, the IC shuts down the power MOSFET.

### Short-Circuit Protection (SCP)

If the load current increases rapidly due to a short-circuit event, the current may exceed the current limit threshold before the control loop can respond. If the current reaches the 8A secondary current limit level, a fast turn-off circuit activates to turn off the power MOSFET. This limits the peak current through the switch, and prevents the input voltage from dropping too much. The total short circuit response time is about 1µs. After the MOSFET has switched off, the part restarts. If the short remains while the device is restarting, the MP5035 regulates the gate voltage to hold the current at the normal current limit level. The IC enters hiccup mode after a 700ms off time.

To avoid damaging the IC due to a large input voltage spike during short-circuit protection (SCP) entry, it is recommended to use a minimum 22µF input capacitor when $V_{IN}$ exceeds 15V. If the input surge voltage is higher than 26V absolute voltage will have risk to damage the IC. To prevent safe operating area (SOA) damage during a high input voltage short-circuit condition, the IC current limit folds back when the power MOSFET's voltage ($V_{DS}$) rises above the typical 11V, and the junction temperature exceeds 110°C.


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### Output Discharge

The MP5035 has a discharge function that provides a resistive discharge path for the external output capacitor. When the part is disabled (VIN UVLO, EN shutdown) and is done in a very limited time.

### Enable (EN)

The MP5035 is enabled when the EN pin is high. The MP5035 is disabled when EN is low. Float the EN pin to shut down the MP5035. There is an internal 2.2MΩ resistor pulling EN down to ground.

EN is clamped internally using a 5.5V Zener diode (see Figure 2). Connecting the EN input to VIN through a pull-up resistor limits the EN input current below 100μA. This prevents damage to the Zener diode.

For example, if $V_{IN}$ is 12V and a 300kΩ pull-up resistor is connected between EN and GND, the Zener diode current can be calculated with the following equation: $I_{ZENER}$ = ((12V - 5.5V) / 300kΩ) - (5.5V / 2.2MΩ) = 19μA.

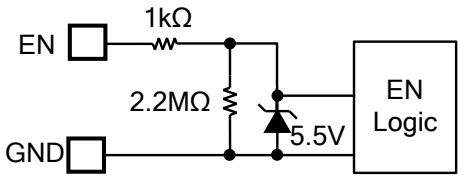



**Figure 2: Zener Diode between EN and GND**

When using a pull-up resistor to set the power-on threshold, avoid using a pull-up resistor with an insufficient resistance, as this can cause the operating quiescent current to increase.

### Thermal Shutdown (Auto-Retry)

Thermal shutdown prevents the chip from operating at exceedingly high temperatures. If the silicon die temperature exceeds 175°C, the entire chip shuts down. Once the temperature drops below its lower threshold (typically 125°C), the chip is enabled after a 700ms delay.


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# APPLICATION INFORMATION

## Setting the Current Limit

The MP5035 current limit value should exceed the normal maximum load current to allow for tolerances in the current-sense value. The current limit is a function of the external current limit resistor. Table 1 lists examples of typical current limit values and their respective resistor values.

**Table 1: Typical Current Limits vs. Current Limit Resistors** (8)

| $R_{LIMIT}$ | 22kΩ | 5.6kΩ | 1.5kΩ | 549Ω |
|---|---|---|---|---|
| $I_{LIMIT}$ (A) | 0.05 | 0.2 | 0.75 | 2 |

**Note:**

8) The current limits in Table 1 are typical values for the reference design.

Figure 3 shows the relationship between the current limit and $R_{LIMIT}$.

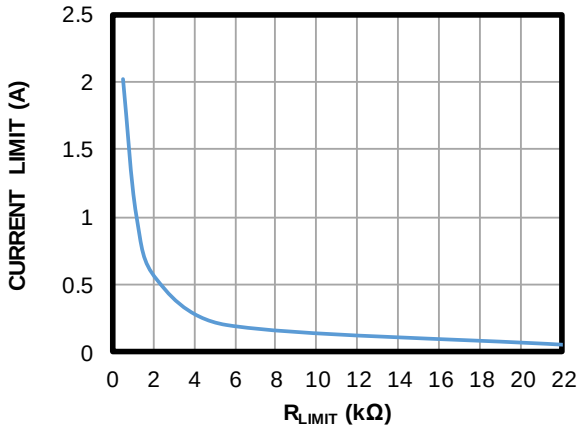



**Figure 3: Current Limit vs. Current Limit Resistor**

The MP5035 current limit can be programmed from 0.05A to 2A via the current limit resistor ($R_{LIMIT}$). It is recommended to use a 1% precision resistor for higher current limit accuracy.

## Setting the Soft-Start Time

The soft-start time ($t_{SS}$) is related to the dV/dt slew rate and the input voltage. $t_{SS}$ can be calculated with Equation (3):

$$t_{SS}(ms) = \frac{V_{IN}(V)}{dV/dt\ (V/ms)} \quad (3)$$

The dV/dt slew rate is controlled by the external DV/DT capacitor setting. When DV/DT is floating, the dV/dt slew rate is 2V/ms.

For cases with an external DV/DT capacitor, the dV/dt slew rate can be calculated with Equation (4):

$$dV/dt\ (V/ms) = \frac{6.5(\mu A) \times 30}{C_{DV/DT}(nF)} \quad (4)$$

For example, when the external DV/DT capacitor is 47nF, the dV/dt slew rate is 4.2V/ms.

## Design Example

Table 2 shows a design example following the application guidelines for particular specifications.

**Table 2: Design Example**

| $V_{IN}$ (V) | 2.9 to 22 |
|---|---|
| Current limit (A) | 2 |
| DV/DT slew rate (V/ms) | 2 |

Figure 5 on page 14 shows the detailed application circuit. The Typical Performance Characteristics section starting on page 5 shows the typical performance and circuit waveforms. For more detailed device applications, refer to the related evaluation board datasheet.


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## PCB Layout Guidelines

Efficient layout is critical for stable operation. For the best results, refer to Figure 4 and follow the guidelines below:

1. Place the high-current paths (VIN and VOUT) close to the device using short, direct, and wide traces.
2. Place the input capacitors close to the VIN and GND pins.
3. Connect the VIN and VOUT pads to the large VIN and VOUT planes to improve thermal performance.
4. Place a current-limit resistor close to ILIMIT.
5. Place a DV/DT capacitor close to the DV/DT pin.

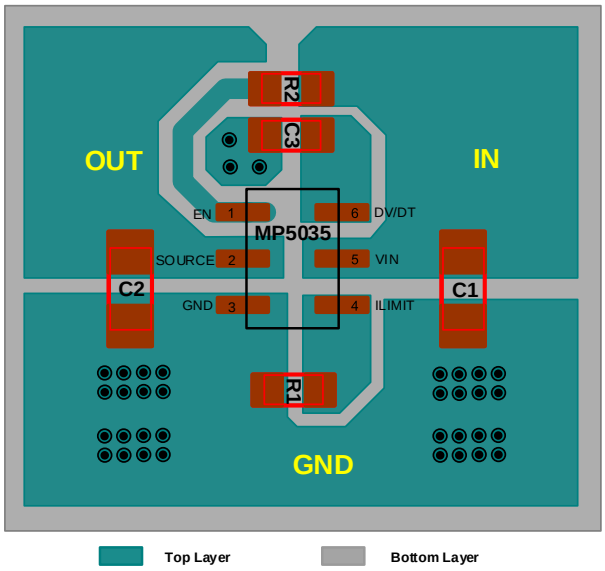



**Figure 4: Recommended PCB Layout**


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## TYPICAL APPLICATION CIRCUIT

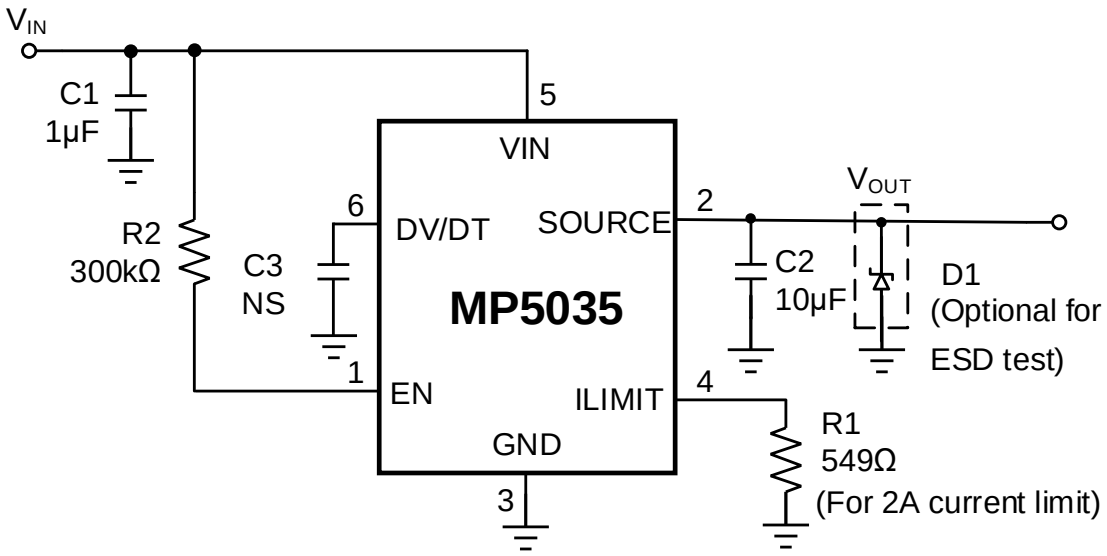



**Figure 5: Typical Application Circuit** (9)

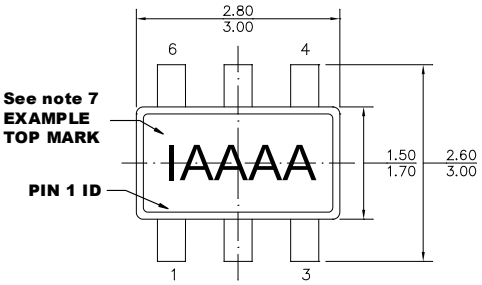
**Note:**

9) A TVS diode (D1) can be used for system ESD tests. D1 is an optional component.

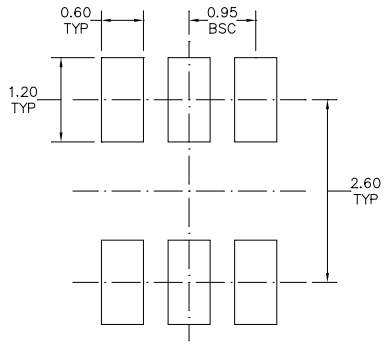

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# PACKAGE INFORMATION

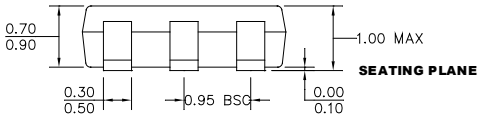
## TSOT23-6



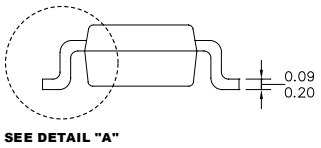

**TOP VIEW**



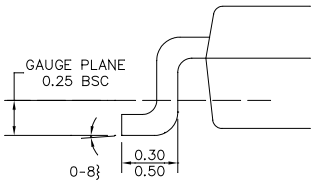

**RECOMMENDED LAND PATTERN**




**FRONT VIEW**




**SIDE VIEW**



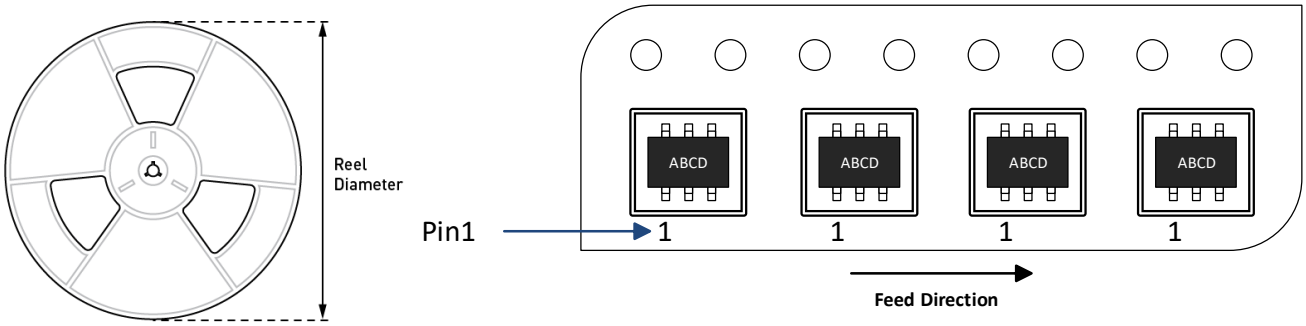

**DETAIL "A"**

**NOTE:**

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSION, OR GATE BURR.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLAS OR PROTRUSION.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMI SHALL BE 0.10 MILLIMETERS MAX.
5) DRAWING CONFORMS TO JEDEC MO-193, VARIATION AE
6) DRAWING IS NOT TO SCALE.
7) PIN 1 IS LOWER LEFT PIN WHEN READING TOP MARK FROM LEFT TO RIGHT, (SEE EXAMPLE TOP MARK)


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## CARRIER INFORMATION




| Part Number | Package Description | Quantity/ Reel | Quantity/ Tube | Reel Diameter | Carrier Tape Width | Carrier Tape Pitch |
|---|---|---|---|---|---|---|
| MP5035GJ-Z | TSOT23-6 | 3000 | N/A | 7in | 8mm | 4mm |


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## REVISION HISTORY

| Revision # | Revision Date | Description | Pages Updated |
|---|---|---|---|
| 1.0 | 09/14/2021 | Initial Release | - |

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