5-A Peak, High Frequency, Dual-Channel, Low-Side Driver

1. Description

The MD18724 high-frequency gate driver is designed to drive both low-side N-Channel MOSFETs with maximum control flexibility of independent inputs.

Each channel can source and sink 5A peak current along with rail-to-rail output capability. Less than 10ns rise and fall time with 2.2nF load decrease the switching loss of MOSFET.

MD18724 has 30ns rising and falling propagation delay which allows the systems operating at high frequency with less delay matching variations. These delays are very suited for applications requiring dual-gate drivers with critical timing, such as synchronous rectifiers. When connecting two channels in parallel to increase current-drive capability, intelligent stack detection circuit is implemented to add extra 15ns dead-time between the two channels to avoid shoot through current without adding external series resistor.

The inputs can handle -10V to 26V PWM, which increases robustness against ringing from gate transformer and/or parasitic inductance of long routing traces. The thresholds of input PINs are fixed and independent of the VDD supply voltage.

The MD18724 is offered in 3x3 DFN-8, SOP-8, EMSOP-8 packages.

2. Applications

- Power Supplies for Telecom, Datacom, and 48V to 72V Battery Powered Systems
- Switch-Mode Power Supplies
- Motor Control, Solar Power

3. Features

- 4.5V to 26V VDD Operating Range, 28V ABS MAX
- Input Pins Can Tolerate -10V to +26V, and are Independent of Supply Voltage Range
- Operating Switching Frequency up to 1MHz
- 5-A Source and Sink Output Peak Currents
- Less than 10ns Rise and Fall Time with 2.2nF Load.
- Fast Propagation Delay (30ns Typical)
- Excellent Propagation Delay Matching (1ns Typical)
- TTL and CMOS Compatible Inputs
- Symmetrical Input Thresholds for Channel A and Channel B
- Industry-standard-compatible Pinout
- Available in 3x3 DFN-8, SOP-8, EMSOP-8 Packages
- Specified from -40°C to 140°C

4. Typical Application

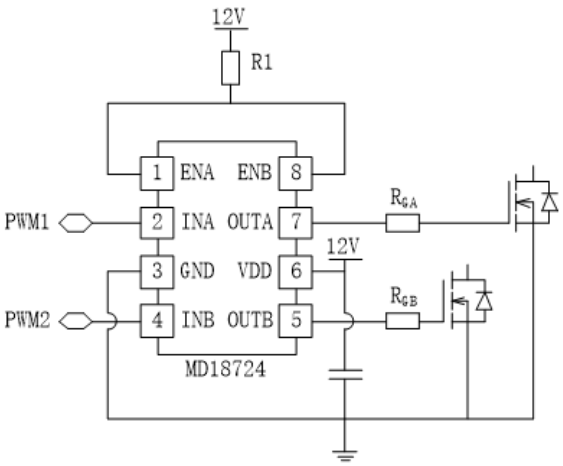


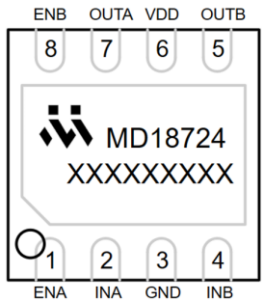
Figure 1 Typical Application Diagram

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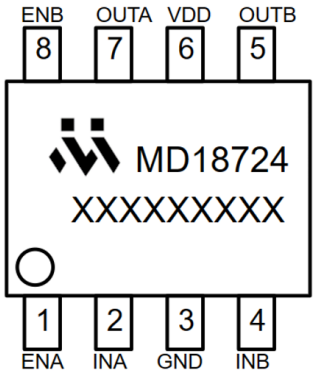
5. Order Information

Order Code	Package	Pins	SPQ (pcs)
MD18724XDB	3x3 DFN-8	8	3000
MD18724XAB	SOP-8	8	4000
MD18724XAE	EMSOP-8	8	4000

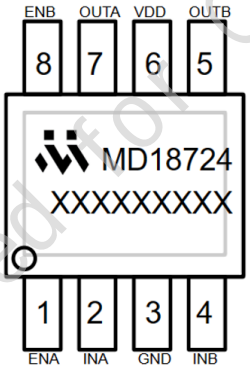
6. Package Reference and Pin Functions



XXXXXXXXX: Lot code
3x3 DFN-8
MD18724XDB



XXXXXXXXX: Lot code
SOP-8
MD18724XAB



XXXXXXXXX: Lot code
EMSOP-8
MD18724XAE

Pin #	Name	Description
1	ENA	Enable input for Channel A: ENA biased LOW disables Channel A output regardless of INA state, ENA biased HIGH or floating enables Channel A output
2	INA	Input of Channel A
3	GND	Negative supply for the device that is generally grounded. All signals of the device are referenced to this ground
4	INB	Input of Channel B
5	OUTB	Output of Channel B
6	VDD	Positive gate drive supply. Locally decouple to VSS using low ESR/ESL capacitor located as close to the device as possible
7	OUTA	Output of Channel A
8	ENB	Enable input for Channel B: ENB biased LOW disables Channel B output regardless of INB state, ENB biased HIGH or floating enables Channel B output

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7. Specifications

7.1 Absolute maximum ratings (1)

VDD .....-0.3V to +28V
INA, INB, ENA, ENB.....-10V to +28V
OUTA, OUTB DC .....-0.3V to VDD+0.3V
Repetitive pulse (2) .....-2V to VDD+0.3V
Repetitive pulse (3) .....-5V to VDD+0.3V
Output continuous source/sink current 0.3A
Junction Temperature .....150℃
Lead temperature (solder) .....260℃
Storage temperature .....-65℃ to 150 ℃

7.2 Recommend operation conditions (4)

VDD.....-0.3V to +28V
INA, INB, ENA, ENB.....-10V to +28V
Maximum junction temp. (T_J) .....+140℃

7.3 Thermal Resistance (5) θ_{JA} θ_{JC}

3 ×3 DFN-8.....64.0 37.8℃/W
SOP-8 .....130.9 80.0℃/W
EMSOP-8.....65.6 71.8℃/W

Notes:

(1) Exceeding these ratings may cause permanent damage to the device.

(2) Repetitive pulse ≤200ns. Verified at bench characterization.

(3) Repetitive pulse ≤100ns. Verified at bench characterization.

(4) The device is not guaranteed to function outside of its operating conditions.

(5) Measured on JEDEC, 1S0P PCB.

7.4 ESD Ratings

		Value	Units
Electrostatic discharge V_{ESD}	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins (1)	±3000	V
	Charged device model (CDM), per JEDEC specification JESD22-C101, all pins (2)	±1000	V

Notes:

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

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7.5 Electrical Characteristics

VDD=12V, T_A=T_J=-40°C to 140°C, 1uF capacitor from V_{DD} to GND. unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Supply Currents						
VDD Start current	$I_{DD\ (off)}$	VDD = 3.4V INA = INB = VDD	40	70	100	uA
		VDD = 3.4V INA = INB = GND	20	40	60	uA
Inputs(Ina, Inb, Ena, Enb)						
Input voltage rising threshold	V_{ITH}		2.25	2.4	2.55	V
Input voltage falling threshold	V_{ITL}		0.65	0.8	0.95	V
Input voltage hysteresis	V_{ITHYS}		1.45	1.6	1.75	V
Undervoltage Lockout						
VDD rising threshold	V_{DDR}		4.0	4.3	4.6	V
VDD falling threshold	V_{DDF}		3.65	3.85	4.05	V
VDD threshold hysteresis	V_{DDHYS}		0.25	0.45	0.75	V
Outputs (Outa, Outb)						
Sink/Source peak current	I_{SNK} /I_{SRC}	C_{LOAD} = 0.22uF, F_{SW} = 1kHz		±5		A
High output voltage	V_{OH}	I_{OUT} = -10mA	VDD -20	VDD -10		mV
Low output voltage	V_{OL}	I_{OUT} = 10mA		8	16	mV
Output pullup resistance	R_{OH}	I_{OUT} = -10mA	0.5	1	2	Ω
Output pulldown resistance	R_{OL}	I_{OUT} = 10mA	0.4	0.8	1.6	Ω
Propagation Delays						
IN to OUT turn-on propagation delay	T_{D1}	C_{LOAD}=2.2nF, 5V input pulse	20	30	45	ns
IN to OUT turn-off propagation delay	T_{D2}	C_{LOAD}=2.2nF, 5V input pulse	20	30	45	ns
EN to OUT turn-on propagation delay	T_{D3}	C_{LOAD}=2.2nF, 5V EN pulse	20	30	45	ns
EN to OUT turn-off propagation delay	T_{D4}	C_{LOAD}=2.2nF, 5V EN pulse	20	30	45	ns
Delay matching between 2 channels	t_M	INA = INB, OUTA and OUTB at 50% transition point		1	4	ns
Output Rise And Fall Time						
Rise time	t_R	C_{LOAD}=2.2nF, from 10% to 90%		9.6	19	ns
Fall time	t_F			6.8	11	ns
Miscellaneous						
Minimum input pulse width that changes the output				20	30	ns

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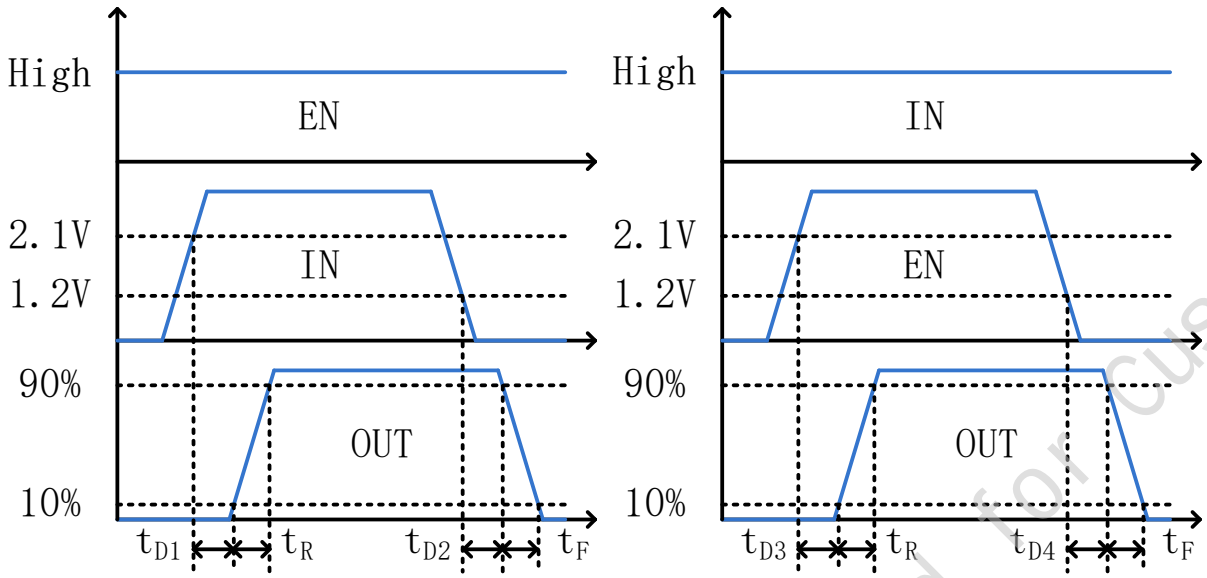


Figure 2 Timing Diagram

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7.6 Typical Characteristics

VDD=3.4V, C_{L_OUTA}= C_{L_OUTB}=470pF

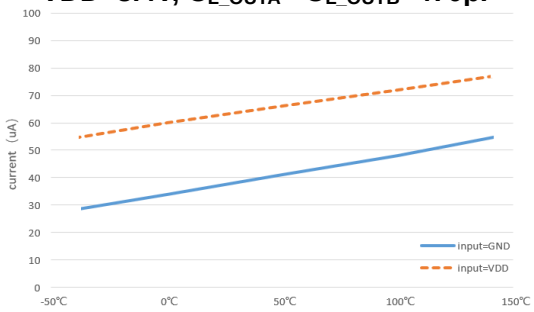


Figure 3 VDD Start Current vs Temperature

VDD=12V, f_{sw}=500kHz, C_{L_OUTA}= C_{L_OUTB}=470pF

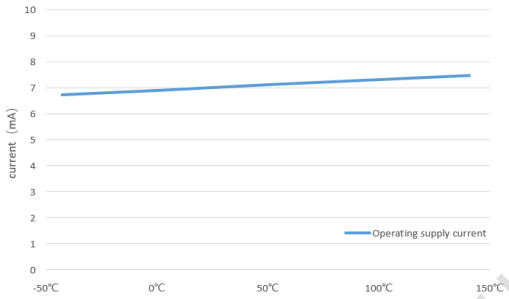


Figure 4. Operating Supply Current vs Temperature
(Outputs Switching)

VDD=12V, C_{L_OUTA}= C_{L_OUTB}=470pF

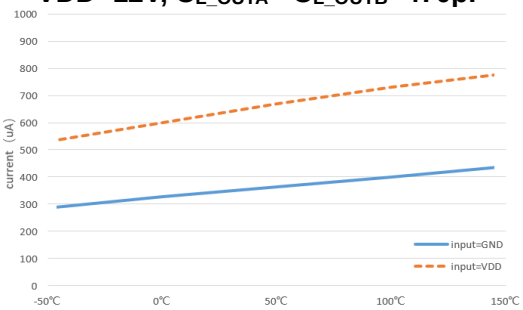


Figure 5. Operating Supply Current vs Temperature
(Outputs No Switching)

VDD=12V, C_{L_OUTA}= C_{L_OUTB}=470pF

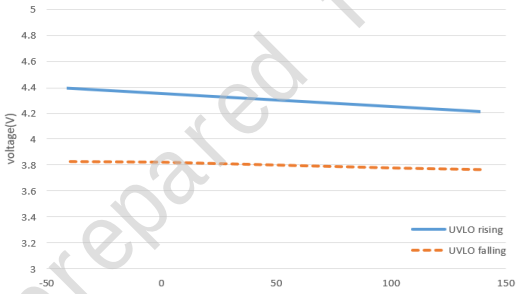


Figure 6. UVLO Threshold vs Temperature

VDD=12V, C_{L_OUTA}= C_{L_OUTB}=2.2nF

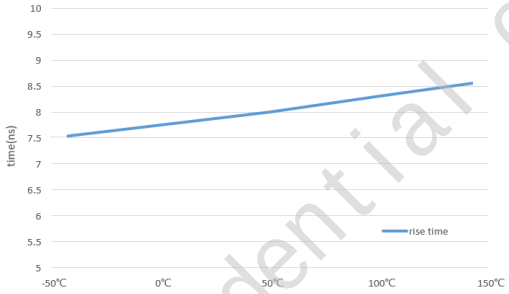


Figure 7. Output Rise Time vs Temperature
25℃, C_{L_OUTA}= C_{L_OUTB}=2.2nF

VDD=12V, C_{L_OUTA}= C_{L_OUTB}=2.2nF

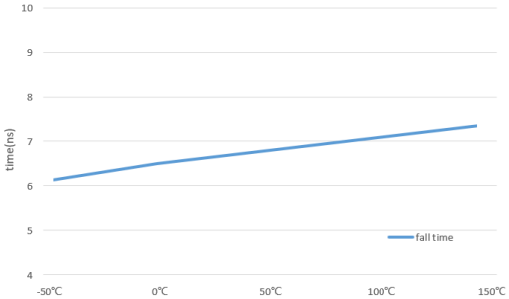


Figure 8. Output Fall Time vs Temperature
VDD=12V, C_{L_OUTA}= C_{L_OUTB}=2.2nF

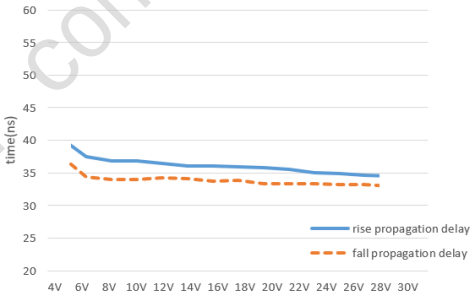


Figure 9. Input to Output Propagation Delays vs VDD Voltage

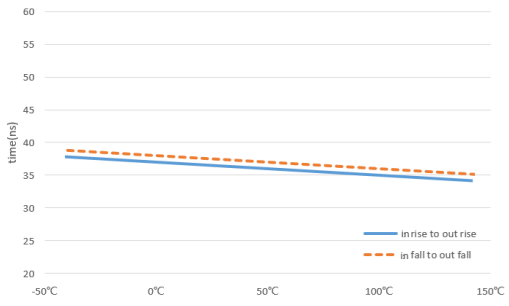


Figure 10. Input to Output Propagation Delay vs Temperature

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25℃, C_{L_OUTA}= C_{L_OUTB}=2.2nF

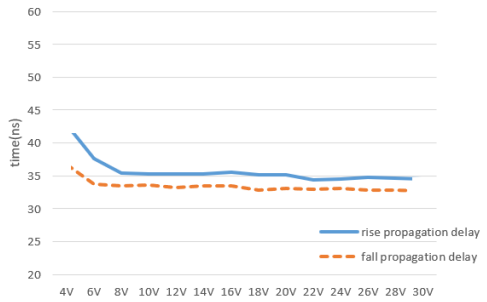


Figure 11. Enable to Output Propagation Delays vs VDD Voltage

VDD=12V, C_{L_OUTA}= C_{L_OUTB}=2.2nF

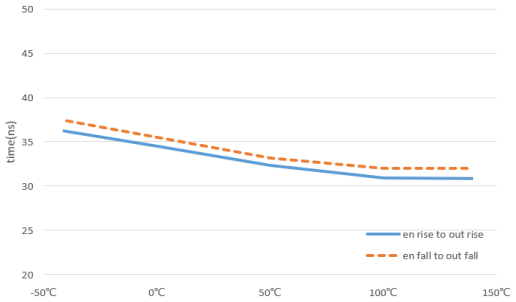


Figure 12. Enable to Output Propagation Delays vs Temperature

25℃, C_{L_OUTA}= C_{L_OUTB}=2.2nF

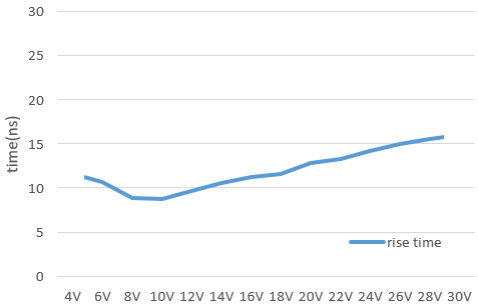


Figure 13. Output Rise time vs VDD Voltage

25℃, C_{L_OUTA}= C_{L_OUTB}=2.2nF

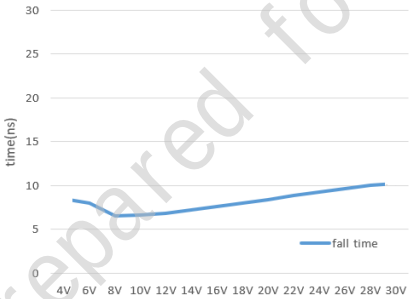


Figure 14. Output Fall time vs VDD Voltage

VDD=12V, C_{L_OUTA}= C_{L_OUTB}=2.2nF

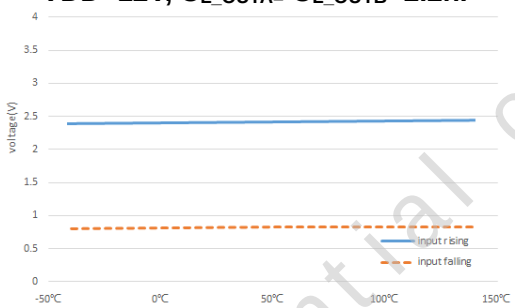


Figure 15. Input Threshold vs Temperature

VDD=12V, C_{L_OUTA}= C_{L_OUTB}=2.2nF

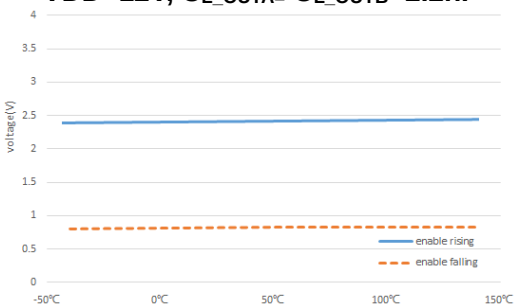


Figure 16. Enable Threshold vs Temperature

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8. Operation

8.1 Overview

The MD18724 high-frequency gate driver is designed to drive both low-side N-Channel MOSFETs with maximum control flexibility of independent inputs.

Each channel can source and sink 5A peak current along with rail-to-rail output capability. Less than 10ns rise and fall time with 2.2nF load decrease the switching loss of MOSFET.

MD18724 has 30ns rising and falling propagation delay which allows the systems operating at high frequency with less delay matching variations. These delays are very suited for applications requiring dual-gate drivers with critical timing, such as synchronous rectifiers. When connecting two channels in parallel to increase current-drive capability, intelligent stack detection circuit is implemented to add extra 15ns dead-time between the two channels to avoid shoot through current without adding external series resistor.

The inputs can handle -10V to 26V PWM, which increases robustness against ringing from gate transformer and/or parasitic inductance of long routing traces. The thresholds of input PINs are fixed and independent of the VDD supply voltage.

The MD18724 is offered in 3x3 DFN-8, SOP-8, EMSOP-8 packages.

8.2 Block Diagram

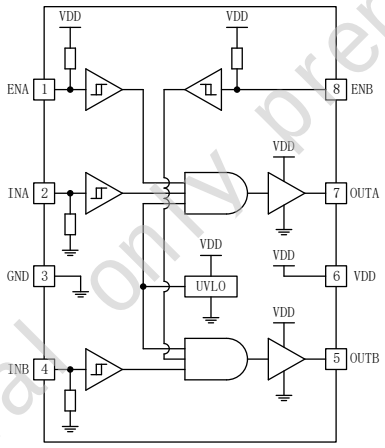


Figure 17 Functional Block Diagram

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8.3 Functional Modes

MD18724 operates in normal mode and UVLO mode. In the normal mode, the output state is dependent on states of the input pins. See as below:

ENA	ENB	INA	INB	OUTA	OUTB
H	H	L	L	L	L
H	H	L	H	L	H
H	H	H	L	H	L
H	H	H	H	H	H
L	L	Any	Any	L	L
Any	Any	X (1)	X (1)	L	L
X (1)	X (1)	L	L	L	L
X (1)	X (1)	L	H	L	H
X (1)	X (1)	H	L	H	L
X (1)	X (1)	H	H	H	H

Note:

(1) X = Floating condition

8.4 VDD power supply and Undervoltage Lockout (UVLO)

MD18724 operates with the supply voltage from 4.5V to 26V. This feature makes MD18724 be capable of driving both MOSFET and IGBT. For the best performance, using a typical 0.1uF decoupling cap as close as possible between VDD and GND pins of MD18724. VDD bypass capacitor (1uF to 10uF) in parallel is also recommended to reduce noise ripple during switching.

MD18724 has internal UVLO protection feature in the VDD supply circuit blocks. When VDD is rising and the voltage is still below UVLO threshold, the outputs stays 'LOW', regardless of the status of the inputs. The UVLO is typically 4.3V with 0.45V hysteresis. This hysteresis prevents false outputs from VDD noise. For example, at powering up, MD18724 output remains 'LOW' until the VDD voltage reaches the VDD rising threshold regardless of the status of inputs. At powering off, MD18724 also outputs 'LOW' after the VDD voltage falls below VDD falling threshold.

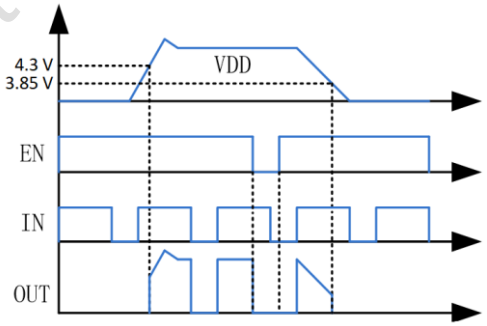


Figure 18 MD18724 operation sequence

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8.5 Input Function

The input pins of MD18724 gate-driver device are based on a TTL and CMOS compatible input-threshold logic. That is independent of the VDD supply voltage. With typically high threshold = 2.4 V and typically low threshold = 0.8 V, the logic level thresholds are conveniently driven by PWM control signals derived from 3.3-V and 5-V digital power-controller devices.

8.6 Output Stage

The output stage of MD18724 features the pull up structure with P-MOS and the pull down structure with N-MOS. The P-MOS provides the pull up capability, when the input is 'HIGH', and the ROH parameter is a DC measurement which is representative of the on-resistance of the P-Channel device. The N-MOS provides the pull-down capability, when the input is 'LOW', the ROL parameter is a DC measurement which is representative of the on-resistance of the N-Channel device.

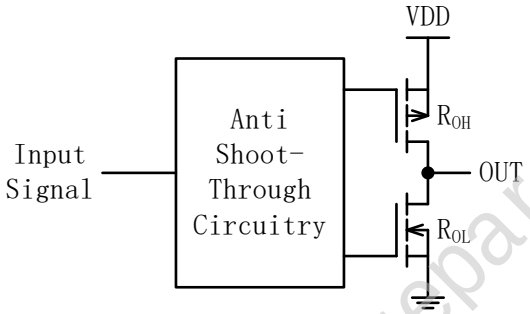


Figure 19 MD18724 Gate Driver Output Structure

Each output stage in MD18724 can supply 5-A peak source and 5-A peak sink current pulses. The output voltage swings between VDD and GND providing rail-to-rail operation by the low on-resistance MOS-output stage which delivers very low drop-out.

The MD18724 device is particularly suited for dual-polarity, symmetrical drive-gate transformer applications where the primary winding of transformer driven by OUTA and OUTB, with inputs INA and INB being driven complementary to each other. This situation is due to the extremely low drop-out offered by the MOS output stage of MD18724, both during high (VOH) and low (VOL) states along with the low impedance of the driver output stage, all of which alleviate concerns regarding transformer demagnetization and flux imbalance. The low propagation delays also ensure accurate reset for high-frequency applications.

For applications that have zero voltage switching during power MOSFET turn-on or turn-off interval, the driver supplies high-peak current for fast switching even though the miller plateau is not present. This situation often occurs in synchronous rectifier applications because the body diode is generally conducting before power MOSFET is switched on.

MD18724 provides excellent output negative voltage handling capability, thanks to its high peak current driving capability and 3kV HBM and 1kV CDM ESD performance.

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8.7 Output Parallel Capability

The MD18724 features 1ns (typical) delay matching between dual channels, which enables dual channel outputs to be paralleled when the driven power device required higher driving capability. For example, in the secondary of hard switching full bridge converter, there are two or more power MOSFETs in parallel to support high current output capability. The parallel power MOSFETs are preferred to be driven by a common gate control signal. By using MD18724, the OUTA and OUTB can be connected to provide the higher driving capability, so does the INA and INB. To support the parallel output, intelligent stack detection is implemented. When two channels are connected, internal circuit can recognize this parallel application and add extra 15ns dead-time to avoid shoot through.

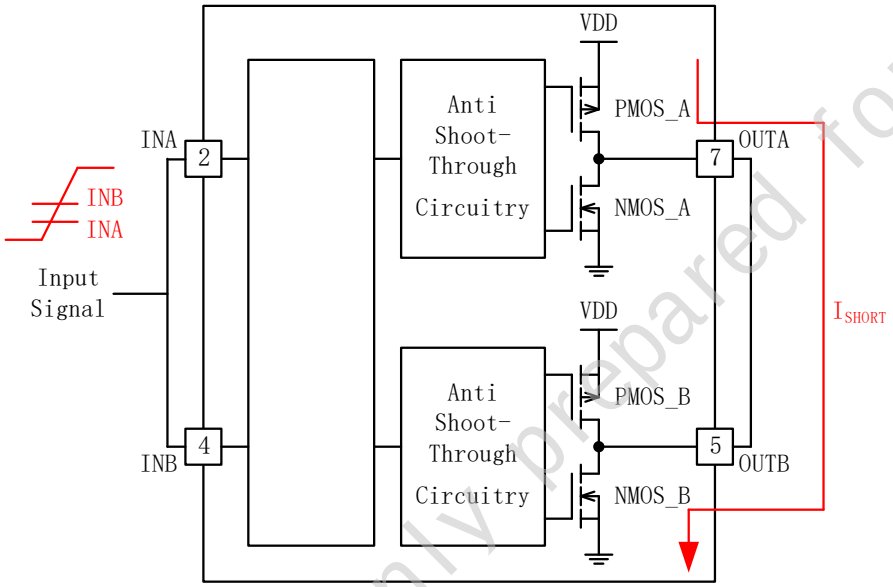


Figure 20. MD18724 Parallel Output Structure

Due to the rising and falling threshold mismatch between INA and INB, shoot through current conduction as shown in Figure 8.4 when directly connecting OUTA and OUTB pins. To avoid the shoot through current, intelligent stack detection is implemented. Extra 15ns dead-time is added between the two channels to cancel the delay between the two channels when slow dv/dt input signals are employed. No extra dead-time is added when the two channels parallel are not detected, so has no influence on propagation delay under normal operation. With the benefit of the intelligent stack detection circuit, MD18724 can support slow input signal slew rate (20V/us or greater) without external gate resistor in series with OUTA and OUTB, so wider application range and lower BOM count is obtained.

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CH1: IN CH2: OUT

Single output driving waveform

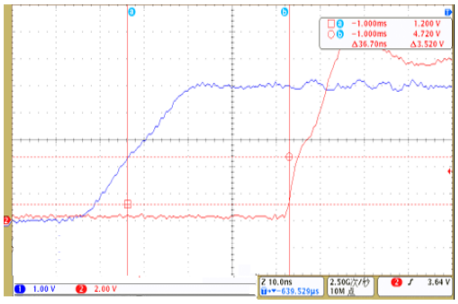


Figure 21. Turn-on propagation delay

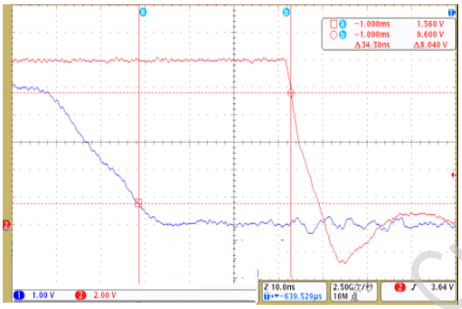


Figure 22. Turn-off propagation delay

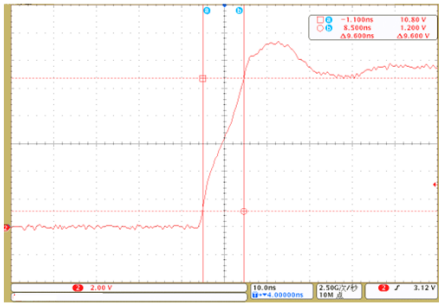


Figure 23. Rise time



Figure 24. Fall time

Dual outputs in parallel driving waveform

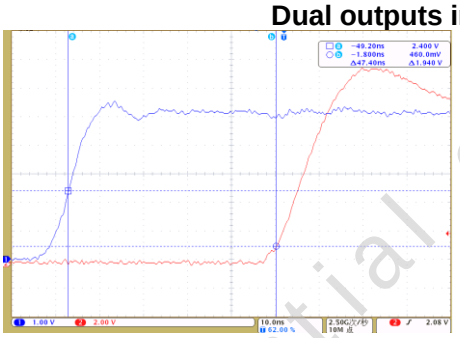


Figure 25. Turn-on propagation delay

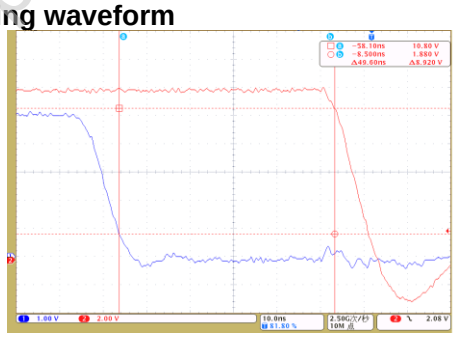


Figure 26. Turn-off propagation delay

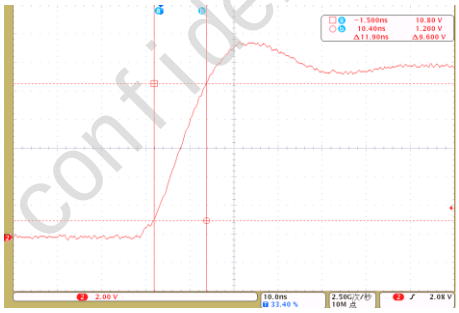


Figure 27. Rise time

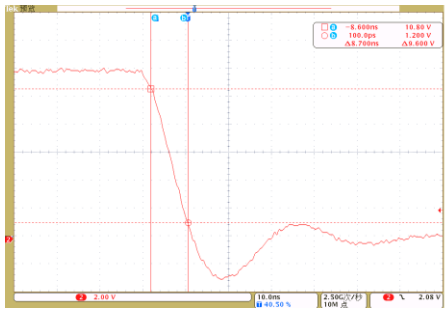


Figure 28. Fall time

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9. Application and Implementation

9.1 Typical Application

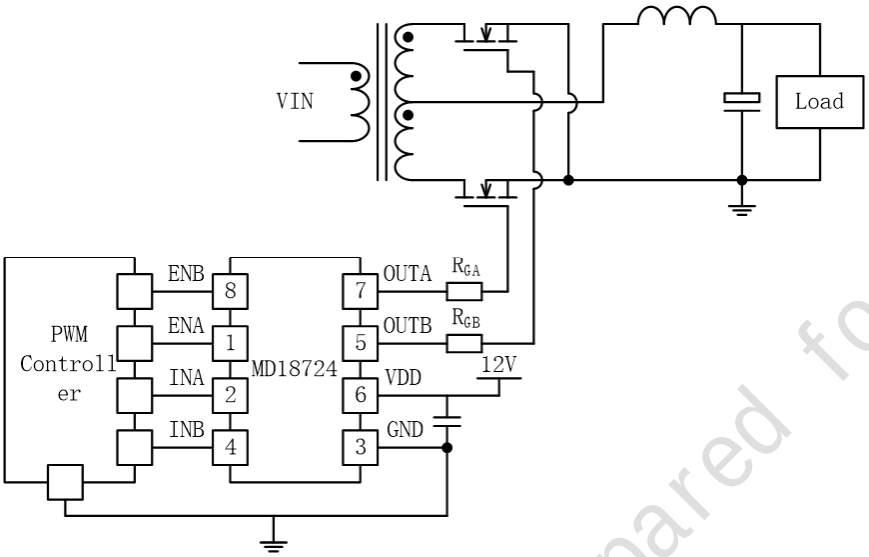


Figure 29 Synchronous Rectification Application

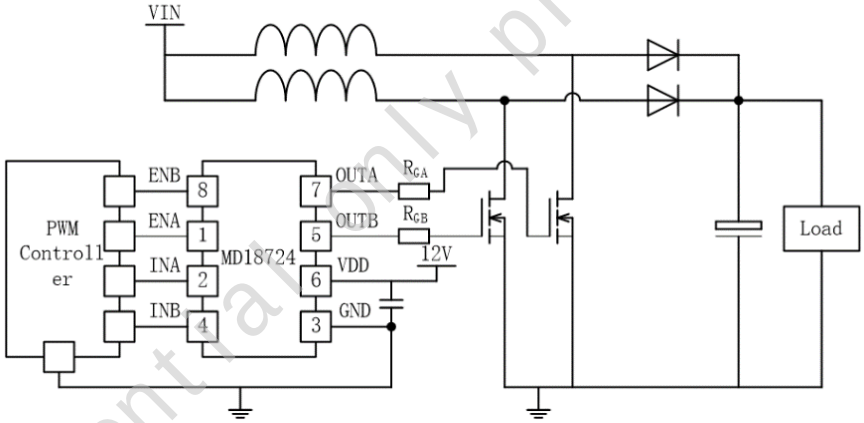


Figure 30. PFC Application

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9.2 Driver Power Dissipation

Generally, the power dissipated in the MD18724 depends on the gate charge required of the power device (Qg), switching frequency, and use of external gate resistors. The MD18724 features extremely low quiescent currents with internal logic to eliminate any shoot-through in the output driver stage, so that the power dissipation within the gate driver is negligible.

When a driver device is evaluated with a discrete capacitive load, calculating the power that is required from the bias supply is simple. The energy that must be transferred from the bias supply to charge the load capacitor is given by Equation 1.

$$E_G = \frac{1}{2} \times C_{LOAD} \times V_{DD}^2 \quad (1)$$

where

C_{LOAD} is load capacitor.

VDD is bias voltage feeding the driver.

There is an equal amount of energy dissipated when the load capacitor is charged. This leads to a total switching power loss of the driver given by Equation 2.

$$P_G = C_{LOAD} \times V_{DD}^2 \times f_{SW} \quad (2)$$

where

fsw is the switching frequency.

The switching load presented by a power MOSFET is converted to an equivalent capacitance by examining the gate charge required to switch the device. This gate charge includes the effects of the input capacitance plus the added charge needed to swing the drain voltage of the power device between the ON and OFF states. Most manufacturers provide specifications that provide the typical and maximum gate charge to switch the device under specified conditions. Using the gate charge Qg, the power that must be dissipated when charging a capacitor is determined by using the Equation 3 to provide Equation 4 for power:

$$Q_G = C_{LOAD} \times V_{DD} \quad (3)$$

$$P_G = C_{LOAD} \times V_{DD}^2 \times f_{SW} = Q_g \times V_{DD} \times f_{SW} \quad (4)$$

To decrease the stress of MOSFET, adding a gate resistor between output of MD18724 and gate of MOSFET, and the power loss of resistor is given by Equation 5.

$$P_{SW} = 0.5 \times Q_g \times V_{DD} \times f_{SW} \times \left(\frac{R_{OL}}{R_{OL}+R_{GATE}} + \frac{R_{OH}}{R_{OH}+R_{GATE}}\right) \quad (5)$$

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10. Layout

10.1 Layout Guidelines

To improve the switching characteristics and efficiency of a design, the following layout rules must be followed.

1) Locate the driver close to the MOSFETs.
2) Locate the VDD-VSS capacitors close to the driver.
3) Connect the VSS pin to thermal pad and use the thermal pad as GND. The GND trace from MD18724 does directly to the source of the MOSFET, but not be in the high current path of MOSFET source current.
4) For system using multiple drivers, the decoupling capacitors need to be located at VDD-VSS for each driver.
5) Avoid placing VDD, INA, INB, ENA, ENB trace close to OUTA, OUTB signals or any other high dV/dT traces that can induce significant noise into the high impedance leads.
6) Use wide trace for INA, INB, ENA, ENB to decrease the influence of switching ringing made by parasitic inductance.
7) For GND, the number of vias must be a consideration of the thermal pad requirements as well as parasitic inductance.

10.2 Layout Example

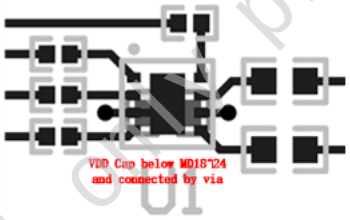


Figure 31. PCB Layout Example for DFN-8 Package

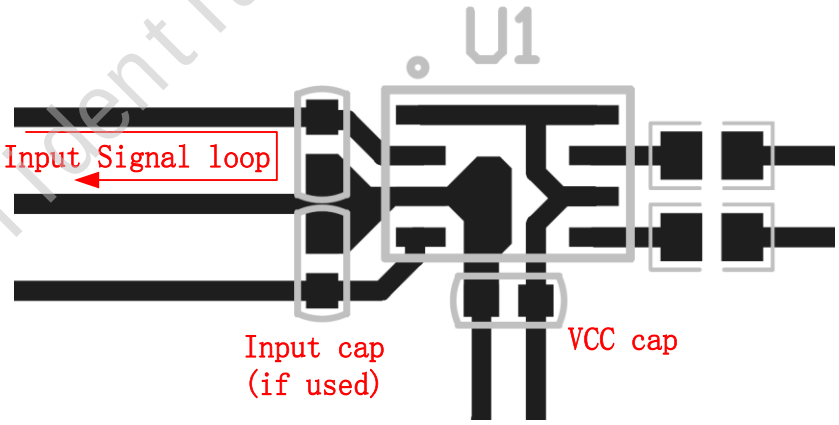


Figure 32. PCB Layout Example for SOP-8 Package

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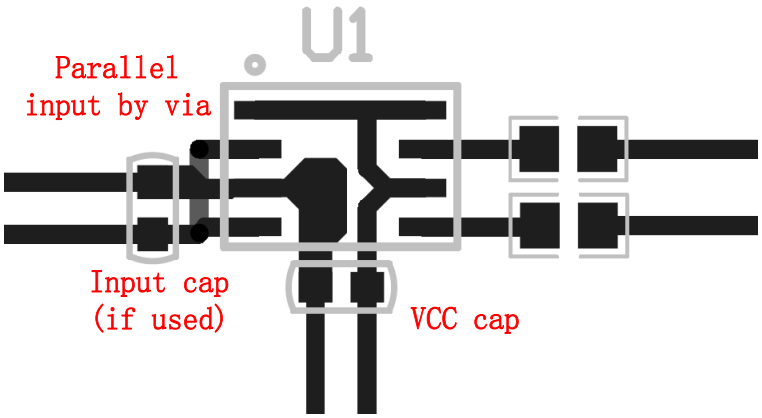


Figure 33. PCB Layout Example with Paralleled Inputs for SOP-8 Package

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11. Mechanical Data and Land Pattern Data

11.1 3X3 DFN-8

11.1.1 Mechanical Data

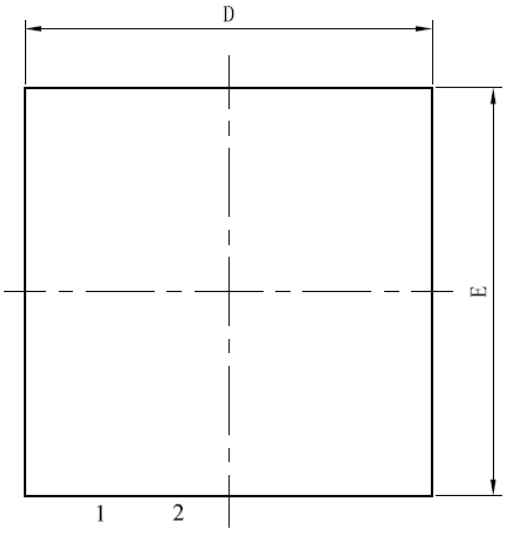


Figure 34. DFN-8 Top View

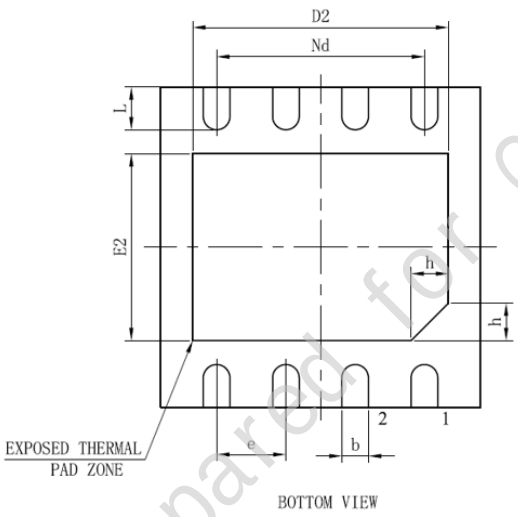


Figure 35. DFN-8 Bottom View

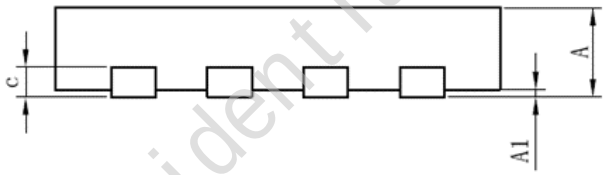


Figure 36. DFN-8 Side View

SYMBOL	Millimeter		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	-	0.02	0.05
b	0.25	0.30	0.35
c	0.18	0.20	0.25
D	2.90	3.00	3.10
D2	2.40	2.50	2.60
e	0.65BSC		
Nd	1.95BSC		
E	2.90	3.00	3.10
E2	1.45	1.55	1.65
L	0.30	0.40	0.50
h	0.20	0.25	0.30

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11.1.2 Land Pattern Data

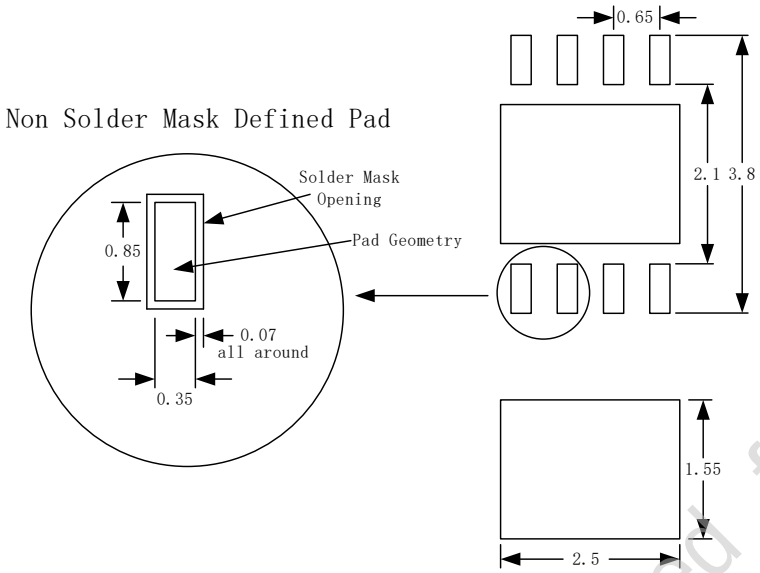
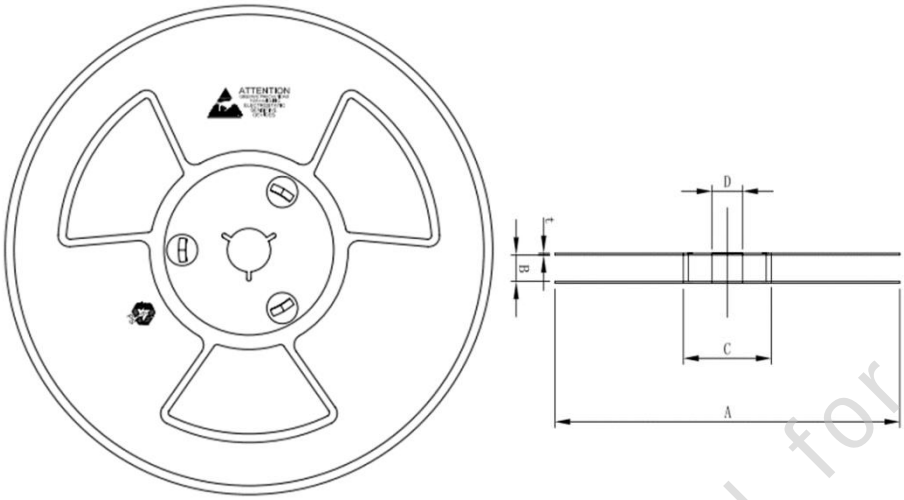


Figure 37. 3x3 DFN-8 Land Pattern Data

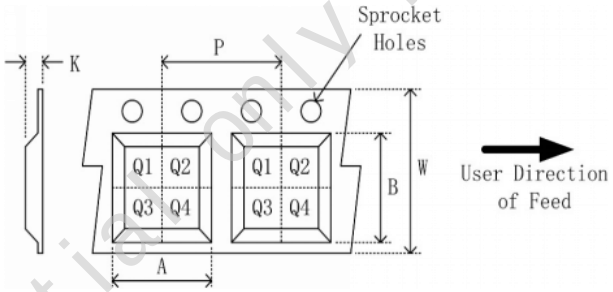
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11.1.3 Tape and Reel Information



Device	Package Type	A (mm)	B (mm)	C (mm)	D (mm)	t (mm)
MD18724XDB	3x3 DFN-8L	329±1	12.4+2.0 −0.0	100±1	13.3±0.3	2.0±0.3

Figure 38. Reel Dimensions

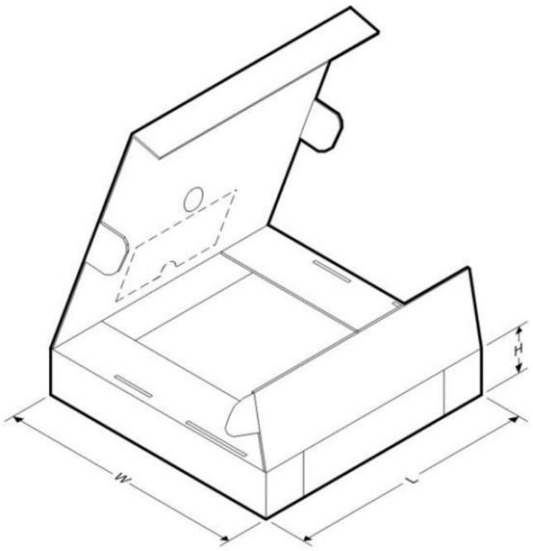


Device	Package Type	Pins	SPQ (pcs)	A (mm)	B (mm)	K (mm)	P (mm)	W (mm)	Pin1 Quadrant
MD18724XDB	3x3 DFN-8L	8	3000	3.3±0.1	3.3±0.1	1.1±0.1	8.0±0.1	12.0±0.3	Q2

Figure 39. Tape Dimensions and Quadrant Assignments for PIN 1 Orientation in Tape

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11.1.4 Tape and Reel Box Dimensions



Device	Package Type	Pins	SPQ (pcs)	Length (mm)	Width (mm)	Height (mm)
MD18724XDB	3x3 DFN-8L	8	3000	360	360	65

Figure 40. Box Dimensions

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11.2 SOP-8

11.2.1 Mechanical Data

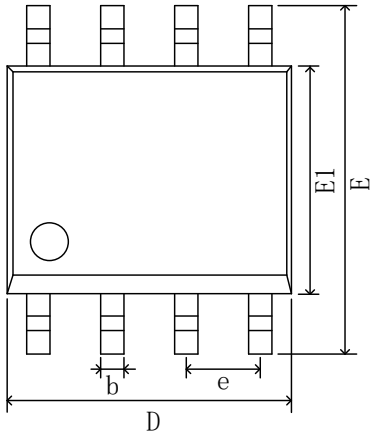


Figure 41. SOP-8 Top View

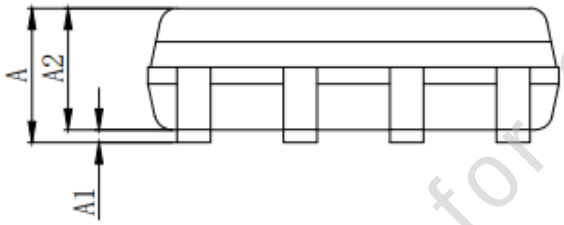


Figure 42. SOP-8 Side View



Figure 43. SOP-8 Side View

SYMBOL	Dimensions In Millimeters	
	MIN	MAX
A	1.30	1.75
A1	0.05	0.25
A2	1.25	1.65
b	0.33	0.51
c	0.20	0.25
D	4.70	5.10
E	5.80	6.20
E1	3.80	4.00
e	1.270(BSC)	
L	0.40	1.27
θ	0°	8°

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11.2.2 Land Pattern Data

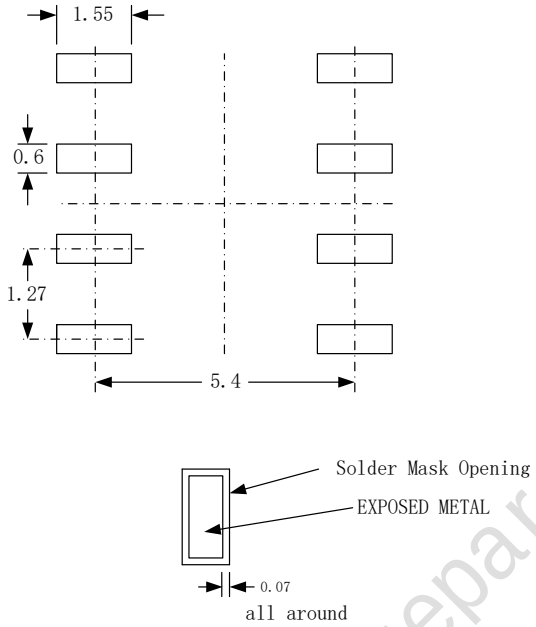


Figure 44. SOP-8 Land Pattern Data

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11.2.3 Tape and Reel Information

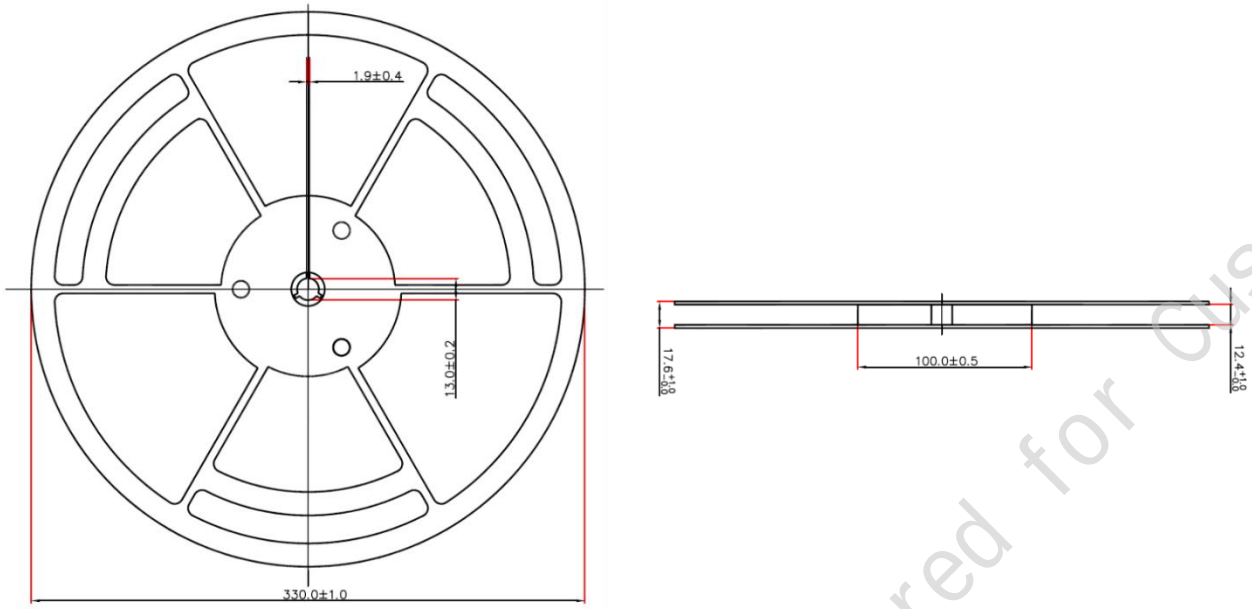
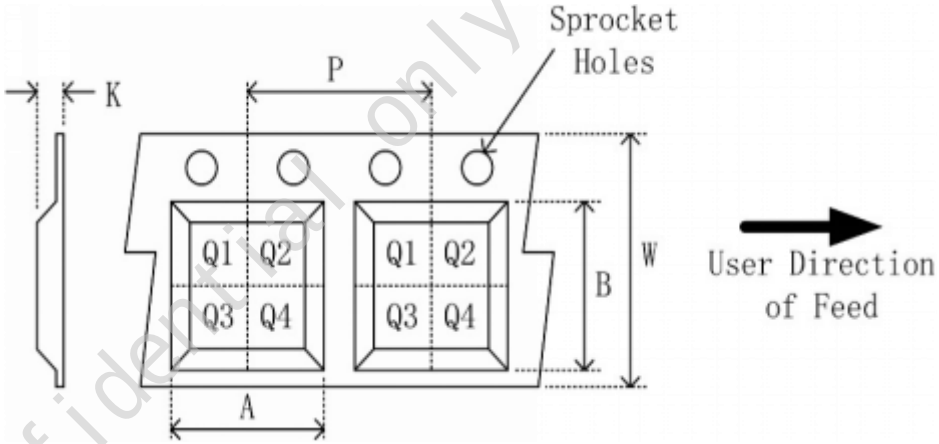


Figure 45. Reel Dimensions

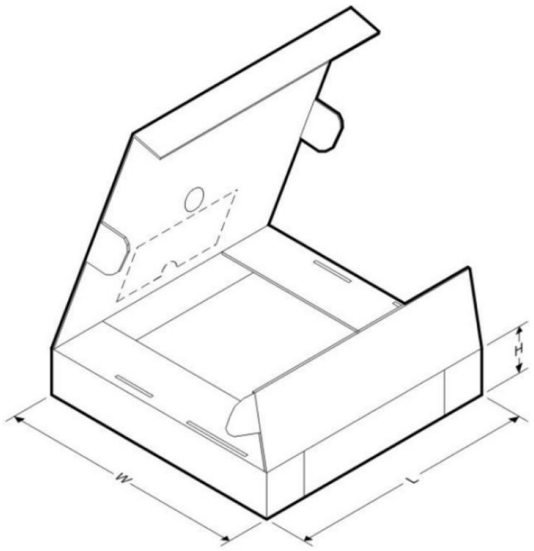


Device	Package Type	Pins	SPQ (pcs)	A (mm)	B (mm)	K (mm)	P (mm)	W (mm)	Pin1 Quadrant
MD18724XAB	SOP	8	4000	6.5±0.1	5.4±0.1	2.0±0.1	8.0±0.1	12.0±0.1	Q1

Figure 46. Tape Dimensions and Quadrant Assignments for PIN 1 Orientation in Tape

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11.2.4 Tape and Reel Box Dimensions



Device	Package Type	Pins	SPQ (pcs)	Length (mm)	Width (mm)	Height (mm)
MD18724XAB	SOP-8	8	8000	360	360	65

Figure 47. Box Dimensions

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11.3 EMSOP-8

11.3.1 Mechanical Data

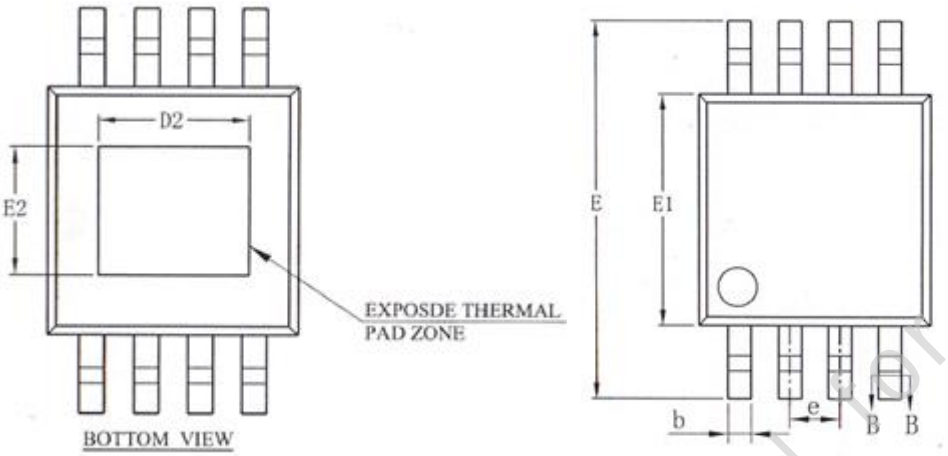


Figure 48. EMSOP-8 Top View

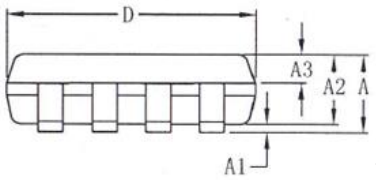


Figure 49. EMSOP-8 Side View

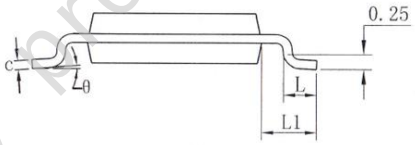


Figure 50. EMSOP-8 Side View

SYMBOL	Millimeter	
	MIN	MAX
A	-	1.10
A1	0.05	0.15
A2	0.75	0.95
b	0.28	0.36
c	0.15	0.29
D	2.90	3.10
E	4.70	5.10
E1	2.90	3.10
e	0.65BSC	
L	0.40	0.70
θ	0°	8°
D2	1.80REF	
E2	1.55REF	

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11.3.2 Land Pattern Data

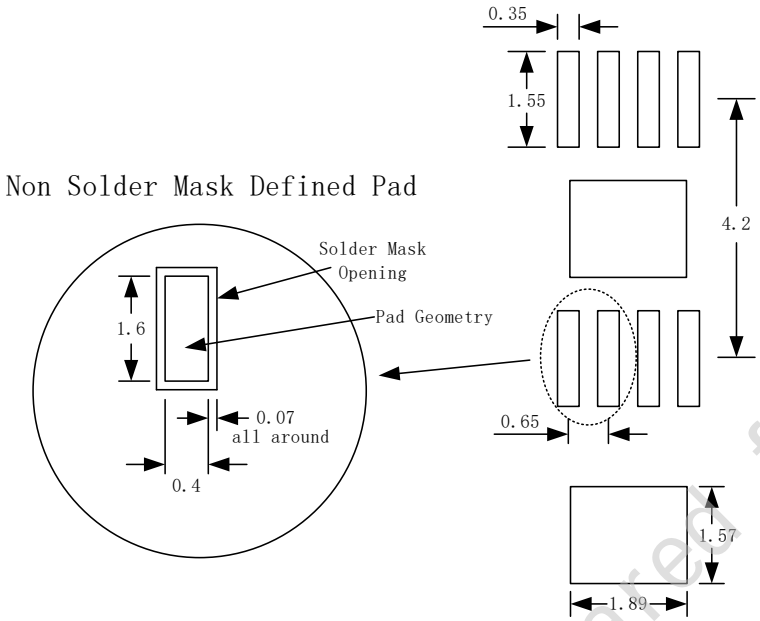
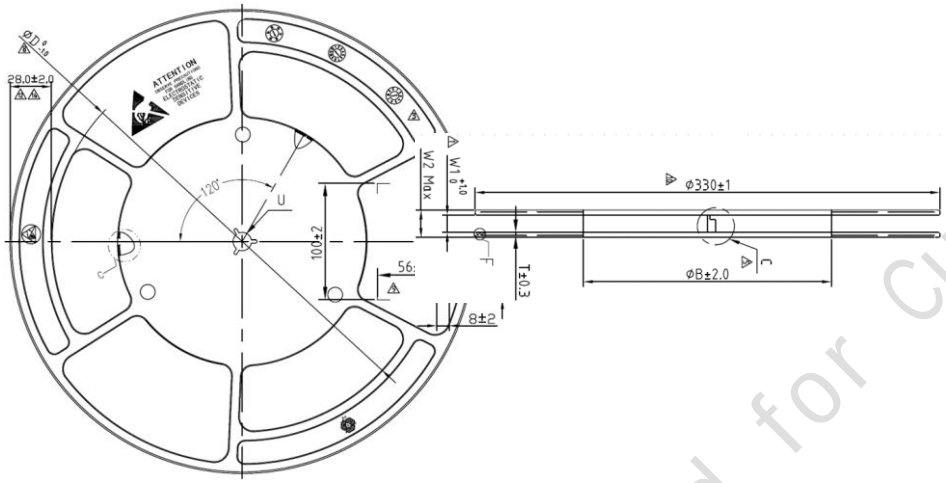


Figure 51. EMSOP-8 Land Pattern Data

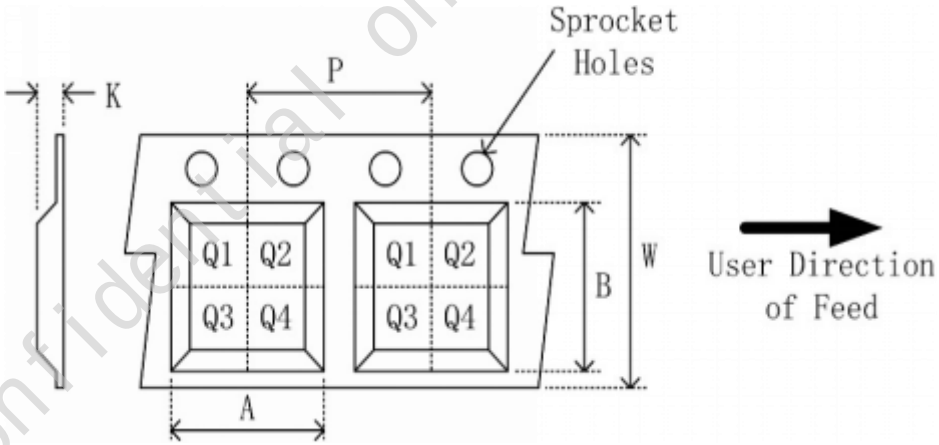
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11.3.3 Tape and Reel Information



⚠2 Specifications (mm)	Suitable for carrier tape widths (mm)	圆盘基本尺寸				
		B (Inner diameter) (mm)	W1 (mm)	W2 Max (mm)	⚠7 T (mm)	⚠8 D (mm)
13”-12× 180	12/12.2	180	12.4	20.4	1.5	275

Figure 52. Reel Dimensions

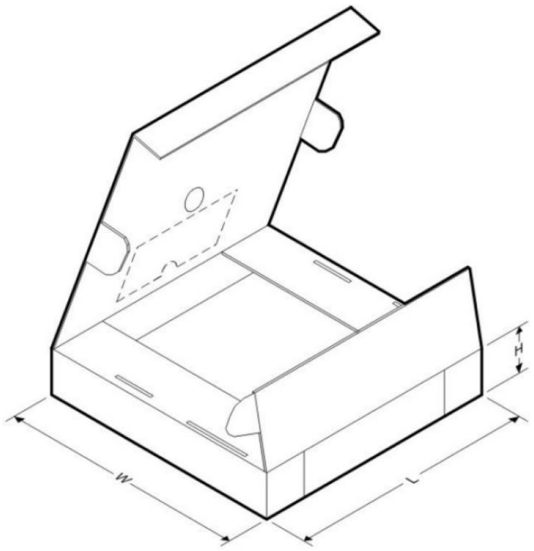


Device	Package Type	Pins	SPQ (pcs)	A (mm)	B (mm)	K (mm)	P (mm)	W (mm)	Pin1 Quadrant
MD18724XAE	EMSOP	8	4000	5.4±0.1	3.4±0.1	1.4±0.1	8.0±0.1	12.0±0.3	Q1

Figure 53. Tape Dimensions and Quadrant Assignments for PIN 1 Orientation in Tape

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11.3.4 Tape and Reel Box Dimensions



Device	Package Type	Pins	SPQ (pcs)	Length (mm)	Width (mm)	Height (mm)
MD18724XAE	EMSOP-8	8	8000	360	360	65

Figure 54. Box Dimensions

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