High Frequency, Single-Channel Low-Side Driver MD18611(4A Source/8A Sink Current) and MD18617(4A Source/4A Sink Current)

1. Description

MD18611/7 high-frequency gate driver is designed to drive the low-side N-Channel MOSFET, IGBT, GaN with maximum control flexibility of independent inputs.

The devices offer superior replacement of NPN and PNP discrete driver (buffer circuit) solutions.

The inputs can handle negative PWM, which increases robustness against ringing from gate transformer and parasitic inductance of long routing traces. The input PINs thresholds are fixed and independent of the VDD supply voltage.

The split output of MD18611 configuration enables easy and independent adjustment of rise and fall times using only two resistors and eliminating the need for an external diode.

2. Typical Applications

- Power Supplies for Telecom, Datacom, and 48V to 72V Battery Powered Systems
- Switch-Mode Power Supplies
- Motor Control, Solar Power

3. Features

- 4.5V to 26V VDD Operating Range, 28V ABS MAX
- Input Pins Can Tolerate -7V to +28V, and are Independent of Supply Voltage Range
- Operating Switching Frequency up to 1MHz
- MD18611 provides 4A Source and 8A Sink Output Peak Currents
- MD18617 provides 4A Source and 4A Sink Output Peak Currents
- Less than 10ns Rise and 5ns Fall Time with 2.2nF Load for MD18611
- Less than 10ns Rise and Fall Time with 2.2nF Load for MD18617
- Fast Propagation Delay (11ns Typical)
- TTL and CMOS Compatible Inputs
- Industry-standard-compatible Pinout
- MD18611 provides SOT23-6 package
- MD18617 provides SOT23-5 package
- Specified from -40°C to 140°C

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4. Typical Application Diagrams

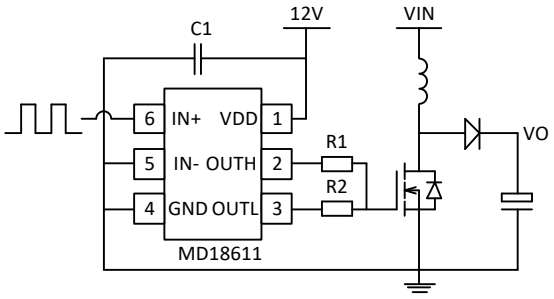


Figure 1. MD18611 Non-Inverting Input

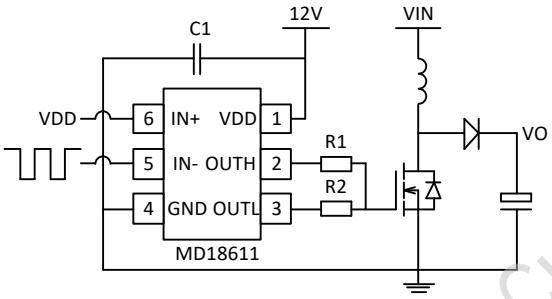


Figure 2. MD18611 Inverting Input

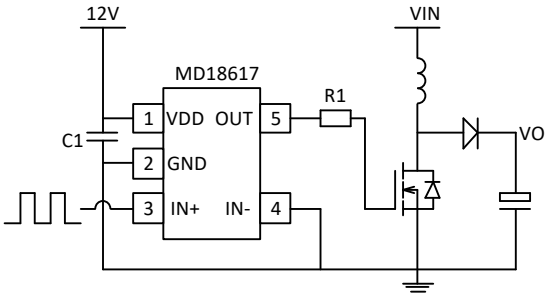


Figure 3. MD18617 Non-Inverting Input

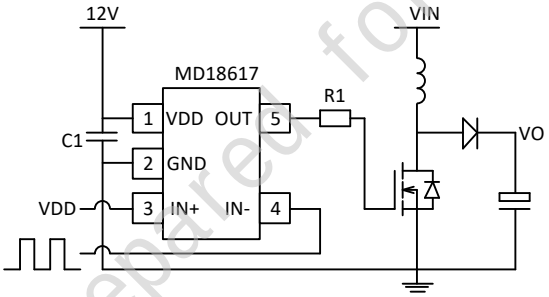


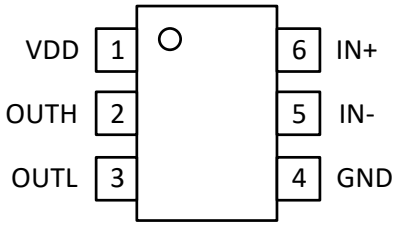
Figure 4. MD18617 Inverting Input

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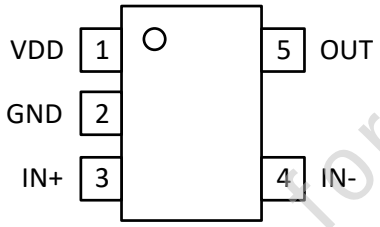
5. Order Information

Order Code	Package	Pins	SPQ (pcs)
MD18611GSA	SOT23-6	6	3000
MD18617GSC	SOT23-5	5	3000

6. Package Reference and pin Functions



MD18611 SOT23-6 (top view)



MD18617 SOT23-5 (top view)

MD18611 pin Number	MD18617 pin Number	Name	Description
1	1	VDD	Positive gate drive supply. Locally decouple to VSS using low ESR/ESL capacitor located as close to the device as possible
2	-	OUTH	Sourcing current output of driver. Connect a resistor between the OUTH pin and the gate of the power switching device to adjust turn-on speed.
3	-	OUTL	Sinking current output of driver. Connect a resistor between the OUTL pin and the gate of the power switching device to adjust turn-off speed.
-	5	OUT	Sourcing/Sinking current output of driver.
4	2	GND	Ground. All signals referenced to this pin.
5	4	IN-	Inverting input. When used in non-inverting configuration, connect the IN– pin to GND to enable output. To disable the output connect the IN– pin to VDD or leave floating.
6	3	IN+	Non-inverting input. When used in inverting configuration, connect the IN+ pin to VDD to enable output. To disable output connect the IN+ pin to GND or leave floating.

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7. Absolute Maximum Ratings (1)

VDD	–0.3V to +28V
IN+, IN-	–7V to +28V
OUTH, OUTL, OUT DC	–0.3V to VDD+0.3V
Repetitive pulse (2)	–2V to VDD+0.3V
Repetitive pulse (3)	–5V to VDD+0.3V
Output continuous source current	0.3A
Output continuous sink current for MD18611	0.6A
Output continuous sink current for MD18617	0.3A
Junction Temperature	150°C
Lead Temperature (Solder)	260°C
Storage Temperature	–65°C to +150°C

8. RECOMMEND OPERATION CONDITIONS (4)

VDD	4.5V to 26V
IN+, IN-	–5V to 26V
Maximum Junction Temp. (T_J)	+140°C

9. THERMAL RESISTANCE (5)

	Θ_{JA}	Θ_{JC}	
SOT23-6	216.7	96.5	°C/W
SOT23-5	216.7	84.7	°C/W

Notes:

(1) Exceeding these ratings may cause permanent damage to the device.

(2) Repetitive pulse ≤200ns. Verified at bench characterization.

(3) Repetitive pulse ≤100ns. Verified at bench characterization.

(4) The device is not guaranteed to function outside of its operating conditions.

(5) Measured on JEDEC, 1S0P PCB.

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10. ESD Ratings

		Value	Units
Electrostatic discharge V_{ESD}	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins (1)	±2000	V
	Charged device model (CDM), per JEDEC specification JESD22-C101, all pins (2)	±1000	V

Notes:

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

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11. Electrical Characteristics

VDD=12V, T_A=T_J=-40°C to 140°C, 1uF capacitor from V_{DD} to GND. unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
SUPPLY CURRENTS						
VDD Start current (VDD=3.4V)	I_{START}	IN+= VDD or GND, IN-=GND	20	57	100	uA
		IN+= VDD or GND, IN-=VDD	16	35	52	uA
Inputs(IN+, IN-)						
Input voltage rising threshold	V_{ITH}	Output high for IN+ Output low for IN-	2.00	2.20	2.40	V
Input voltage falling threshold	V_{ITL}	Output low for IN+ Output high for IN-	1.06	1.21	1.36	V
Input voltage hysteresis	V_{ITHYS}		0.82	0.99	1.16	V
Minimum input pulse width				10	20	ns
Undervoltage Lockout						
VDD rising threshold	V_{DDR}		3.95	4.24	4.46	V
VDD falling threshold	V_{DDF}		3.66	3.93	4.14	V
VDD threshold hysteresis	V_{DDHYS}		0.21	0.31	0.41	V
MD18611 Output						
Sink peak current	I_{SNK}	C_{LOAD} = 0.22uF, F_{SW} = 1kHz		8		A
Source peak current	I_{SRC}	C_{LOAD} = 0.22uF, F_{SW} = 1kHz		4		A
High output voltage	V_{OH}	I_{OUT} = -10mA		11	20	mV
Low output voltage	V_{OL}	I_{OUT} = 10mA		5	10	mV
Output pullup resistance	R_{OH}	I_{OUT} = -10mA		1.1	2	Ω
Output pulldown resistance	R_{OL}	I_{OUT} = 10mA		0.5	1.0	Ω
Rise time	t_R	C_{LOAD} = 2.2nF		9	22	ns
Fall time	t_F	C_{LOAD} = 2.2nF		5	12	ns
MD18617 Output						
Sink peak current	I_{SNK}	C_{LOAD} = 0.22uF, F_{SW} = 1kHz		4		A
Source peak current	I_{SRC}	C_{LOAD} = 0.22uF, F_{SW} = 1kHz		4		A
High output voltage	V_{OH}	I_{OUT} = -10mA		11	20	mV
Low output voltage	V_{OL}	I_{OUT} = 10mA		8.5	17	mV
Output pullup resistance	R_{OH}	I_{OUT} = -10mA		1.1	2	Ω
Output pulldown resistance	R_{OL}	I_{OUT} = 10mA		0.85	1.7	Ω
Rise time	t_R	C_{LOAD} = 2.2nF		9	22	ns
Fall time	t_F	C_{LOAD} = 2.2nF		7	17	ns
Propagation Delays						
turn-on propagation delay	T_{D1}	C_{LOAD}=2.2nF, 5V input pulse	5	11	20	ns
turn-off propagation delay	T_{D2}	C_{LOAD}=2.2nF, 5V input pulse	5	11	20	ns

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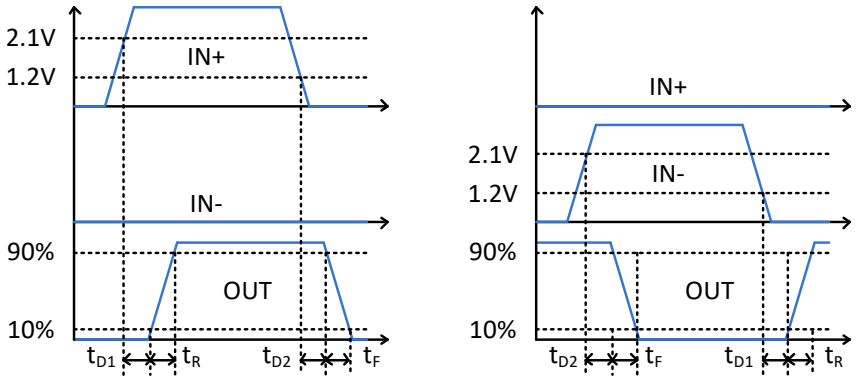


Figure 5. Timing Diagram

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12. Typical Characteristics

VDD=12V, T_A=25°C, unless otherwise noted.

VDD=3.4V

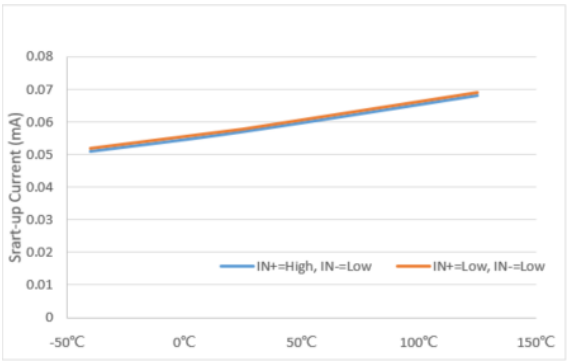


Figure 6. VDD Start Current vs Temperature

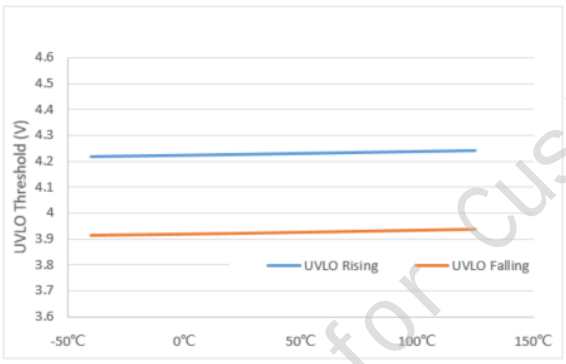


Figure 7. VDD UVLO Threshold Voltage vs Temperature

C_{L_OUTA}= C_{L_OUTB}=470pF

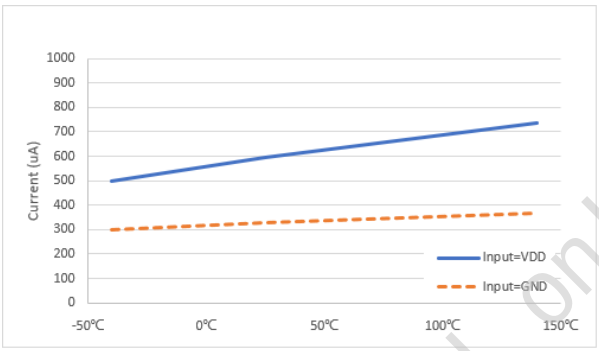


Figure 8. Operating Supply Current vs Temperature (Outputs No Switching)

C_{L_OUTA}= C_{L_OUTB}=470pF

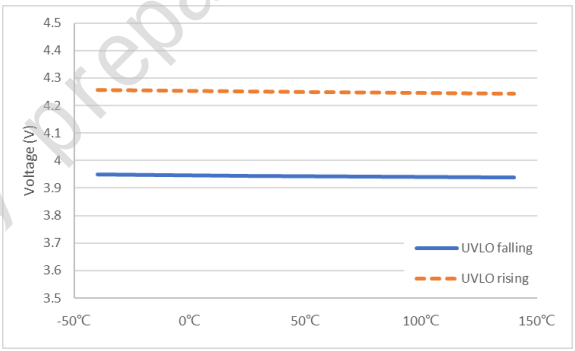


Figure 9. VDD UVLO Threshold vs Temperature

C_{Load}=2.2nF

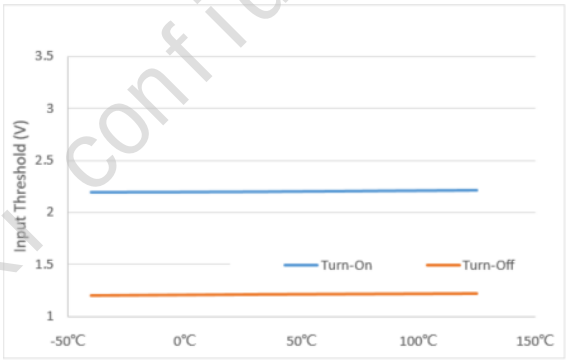


Figure 10. Output Rise Time vs Temperature

C_{Load}=2.2nF

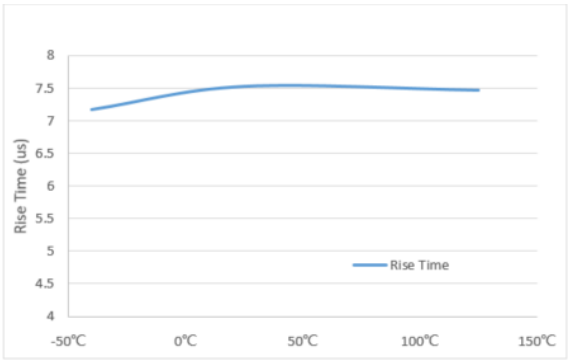


Figure 11. MD18617 Rise Time vs Temperature

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C_{Load}=2.2nF

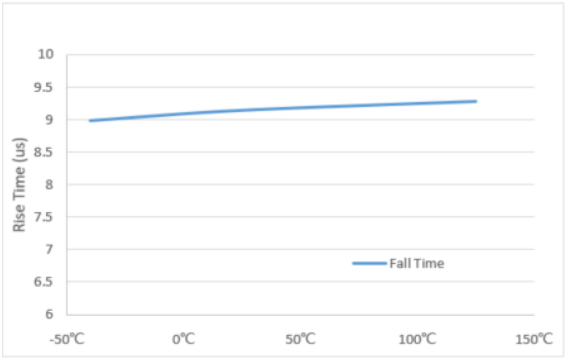


Figure 12. MD18617 Fall Time vs Temperature

C_{Load}=2.2nF

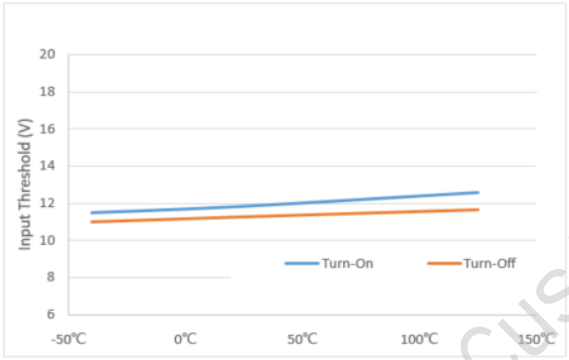


Figure 13. Propagation Delay vs Temperature

C_{Load}=2.2nF

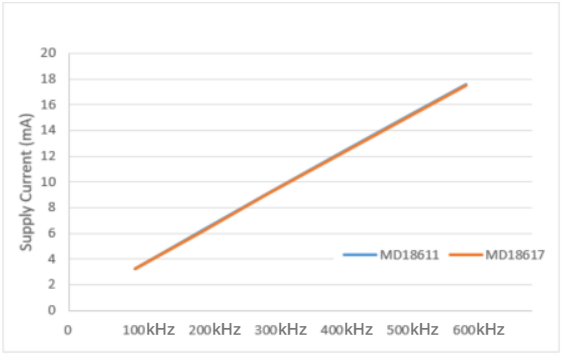


Figure 14. Operating Supply Current vs Frequency

C_{Load}=2.2nF

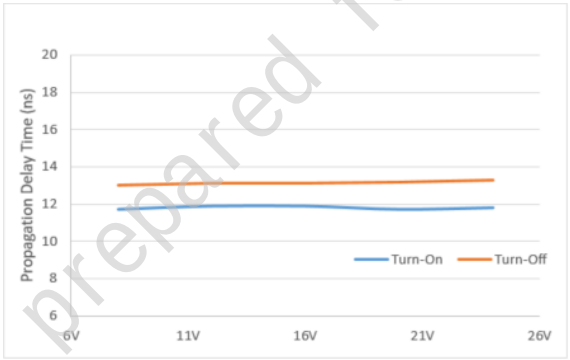


Figure 15. Propagation Delays vs Supply Voltage

C_{Load}=2.2nF

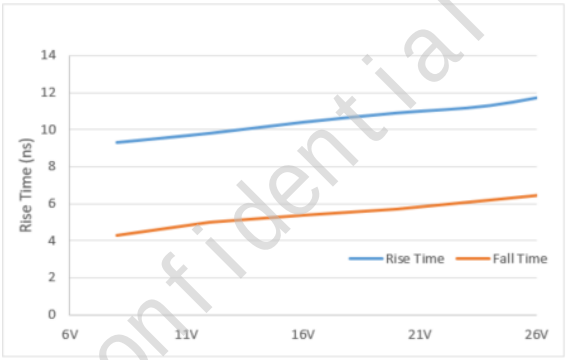


Figure 16. MD18611 Rise & Fall time vs VDD Voltage

C_{Load}=2.2nF

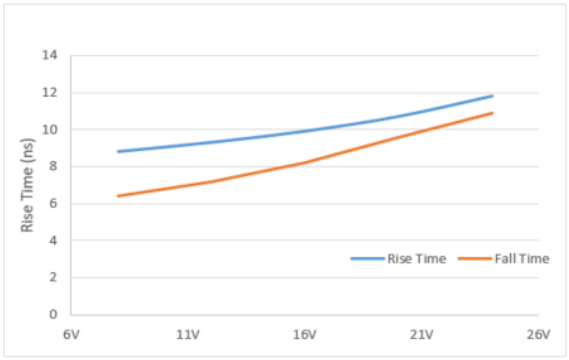


Figure 17. MD18617 Rise & Fall time vs VDD Voltage

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13. Block Diagram

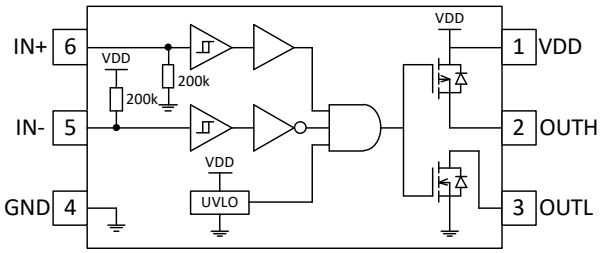


Figure 18. MD18611 Functional Block Diagram

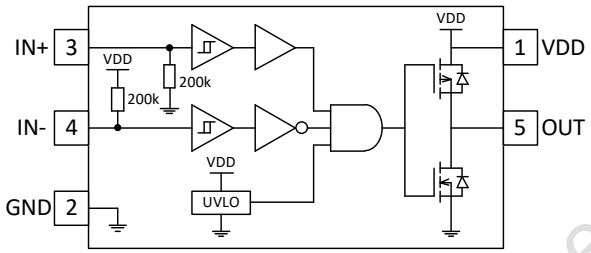


Figure 19. MD18617 Functional Block Diagram

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14. Operation

14.1 Overview

MD18611(7) is a single-channel high-speed low-side driver with supporting up to 26V wide supply voltage. MD18611(source 4A and sink 8A peak current) and MD18617(source 4A and sink 4A peak current) along with the minimum propagation delay 11ns from input to output. The devices support higher switching frequency and driving capability. The 26V rail-to-tail outputs can drive both MOSFET and IGBT.

14.2 Functional Modes

MD18611(7) operates in normal mode and UVLO mode. In the normal mode, the output state is dependent on states of the input pins. See as below:

IN+	IN-	OUTH (MD18611)	OUTL (MD18611)	OUT (MD18617)
L	L	High impedance	L	L
L	H	High impedance	L	L
H	L	H	High impedance	H
H	H	High impedance	L	L
X (1)	Any	High impedance	L	L
Any	X (1)	High impedance	L	L

Note:

(1) X = Floating condition

14.3 VDD power supply and Under Voltage Lockout (UVLO)

MD18611(7) operates with the supply voltage from 4.5V to 26V. This feature makes MD18611(7) be capable of driving both MOSFET and IGBT. For the best performance, Using a typical 0.1uF decoupling cap as close as possible between VDD and GND pins of devices. VDD bypass capacitor (1uF to 10uF) in parallel is also recommended to reduce noise ripple during switching.

MD18611(7) has internal UVLO protection feature In the VDD supply circuit blocks. When VDD is rising and the voltage is still below UVLO threshold, the outputs 'LOW', regardless of the status of the inputs. The UVLO is typically 4.2V with 0.3V hysteresis. This hysteresis prevents VDD from noise problem.

For example, at powering up, MD18611(7) output remains 'LOW' until the VDD voltage reaches the VDD rising threshold regardless of the status of inputs. At powering off, MD18611(7) also outputs low after the VDD voltage falls below VDD falling threshold.

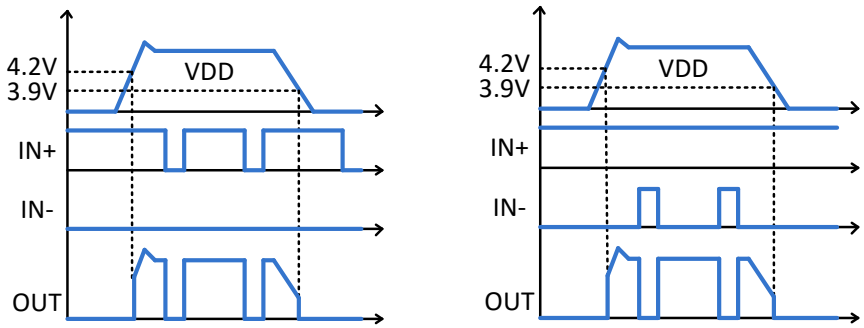


Figure 20. MD18611(OUTH and OUTL tied together) and MD18617 operation sequence

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14.4 Input Function

The input pins of MD18611(7) gate-driver device are based on a TTL and CMOS compatible input-threshold logic. That is independent of the VDD supply voltage. With typically high threshold = 2.1 V and typically low threshold = 1.2 V, the logic level thresholds are conveniently driven by PWM control signals derived from 3.3V and 5V digital power-controller devices.

The device features an important protection function wherein, whenever any of the input pins are in a floating condition, the output of the respective channel is held in the low state. This is achieved using VDD-pull up resistors on all the inverting inputs (IN– pin) or GND-pulldown resistors on all the non-inverting input pins (IN+ pin).

The device also features a dual-input configuration with two input pins available to control the state of the output. The user has the flexibility to drive the device using either a non-inverting input pin (IN+) or an inverting input pin (IN–). The state of the output pin is dependent on the bias on both the IN+ and IN– pins.

14.5 Output Stage

The output stage of MD18611(7) features the pull up structure with P-MOS and the pull down structure with N-MOS. P-MOS provides the pull up capability when Input is 'HIGH', and the ROH parameter is a DC measurement which is representative of the on-resistance of the P-Channel device. N-MOS provides the pull down capability when Input is 'LOW', the ROL parameter is a DC measurement which is representative of the on-resistance of the N-Channel device.

MD18611 can supply 4-A peak source and 8-A peak sink current pulses. MD18617 can supply 4-A peak source and 4-A peak sink current pulses. The output voltage swings between VDD and GND providing rail-to-rail operation, thanks to the MOS-output stage which delivers very low drop-out.

For applications that have zero voltage switching during power MOSFET turn-on or turn-off interval, the driver supplies high-peak current for fast switching even though the miller plateau is not present. This situation often occurs in synchronous rectifier applications because the body diode is generally conducting before power MOSFET is switched on.

MD18611/7 provides excellent output negative voltage handling capability, thanks to its high peak current driving capability and 2kV HBM and 1kV CDM ESD performance.

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15. Application and Implementation

15.1 Typical Application

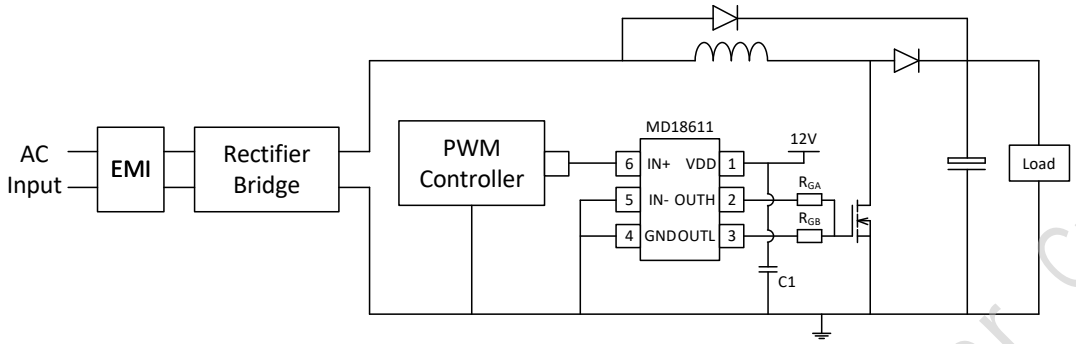


Figure 21. MD18611 PFC Application

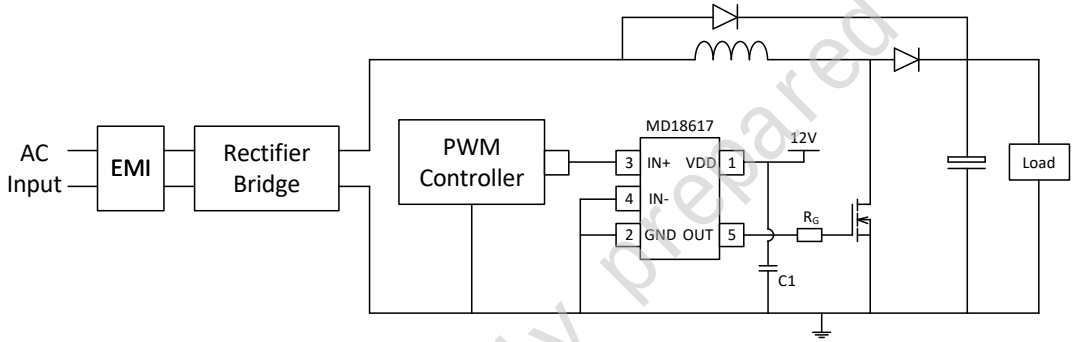


Figure 22. MD18617 PFC Application

15.2 Driver Power Dissipation

Generally, the power dissipated in the MD18611(7) depends on the gate charge required of the power device (Qg), switching frequency, and use of external gate resistors. The MD18611(7) features very low quiescent currents and internal logic to eliminate any shoot-through in the output driver stage, their effect on the power dissipation within the gate driver is negligible.

When a driver device is tested with a discrete, capacitive load calculating the power that is required from the bias supply is fairly simple. The energy that must be transferred from the bias supply to charge the capacitor is given by Equation 1.

$$E_G = \frac{1}{2} \times C_{LOAD} \times V_{DD}^2 \quad (1)$$

where

CLOAD is load capacitor

VDD is bias voltage feeding the driver

There is an equal amount of energy dissipated when the capacitor is charged. This leads to a total power loss given by Equation 2.

$$P_G = C_{LOAD} \times V_{DD}^2 \times f_{SW} \quad (2)$$

where

fsw is the switching frequency

The switching load presented by a power MOSFET is converted to an equivalent capacitance by examining

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the gate charge required to switch the device. This gate charge includes the effects of the input capacitance plus the added charge needed to swing the drain voltage of the power device as it switches between the ON and OFF states. Most manufacturers provide specifications that provide the typical and maximum gate charge to switch the device under specified conditions. Using the gate charge Qg, the power that must be dissipated when charging a capacitor is determined which by using the Equation 3 to provide Equation 4 for power:

$$Q_G = C_{LOAD} \times V_{DD} \quad (3)$$

$$P_G = C_{LOAD} \times V_{DD}^2 \times f_{SW} = Q_g \times V_{DD} \times f_{SW} \quad (4)$$

To decrease the stress of MOSFET, adding a gate resistor between output of MD18611(7) and gate of MOSFET, and the power loss of resistor is given by Equation 5.

$$P_{SW} = 0.5 \times Q_g \times V_{DD} \times f_{SW} \times \left(\frac{R_{OL}}{R_{OL}+R_{GATE}} + \frac{R_{OH}}{R_{OH}+R_{GATE}}\right) \quad (5)$$

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16. Layout

16.1 Layout Guidelines

To improve the switching characteristics and efficiency of a design, the following layout rules must be followed.

1) Locate the driver close to the MOSFETs.
2) Locate the VDD-VSS capacitors close to the driver.
3) The GND trace from MD18611(7) does directly to the source of the MOSFET, but not be in the high current path of MOSFET source current.
4) For system using multiple drivers, the decoupling capacitors need to be located at VDD-VSS for each driver.
5) Avoid placing VDD, IN+, IN- trace close to OUTA, OUTB signals or any other high dV/dT traces that can induce significant noise into the high impedance leads.
6) Use wide trace for IN+, IN- to decrease the influence of switching ringing made by parasitic inductance.
7) For GND, the number of vias must be a consideration of the thermal pad requirements as well as parasitic inductance.

16.2 Layout Example

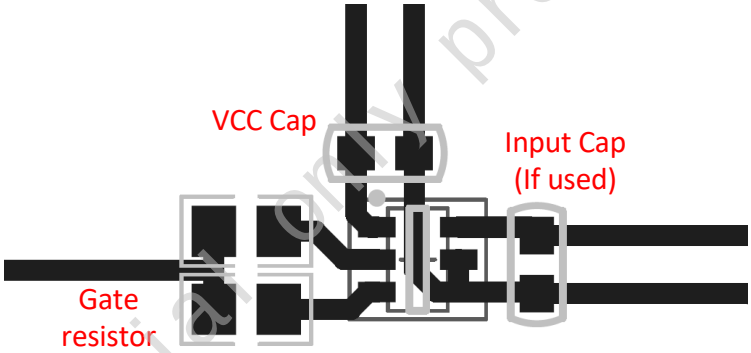


Figure 23. MD18611 PCB Layout Example

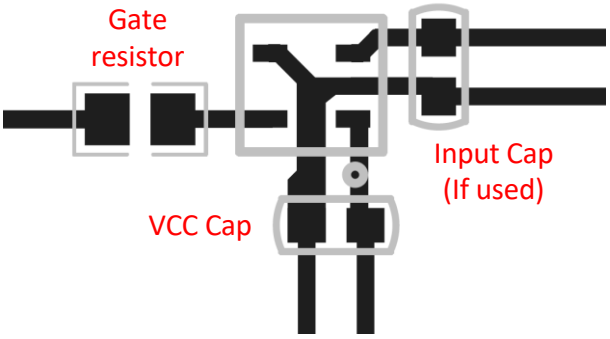


Figure 24. MD18617 PCB Layout Example

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17. Tape and Reel Information

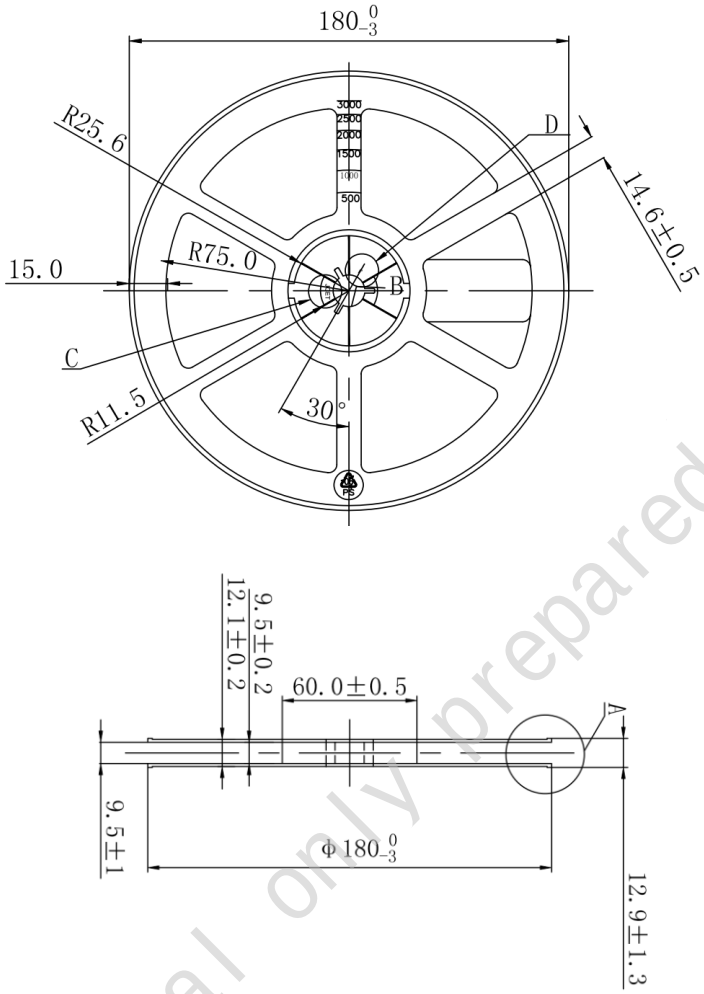
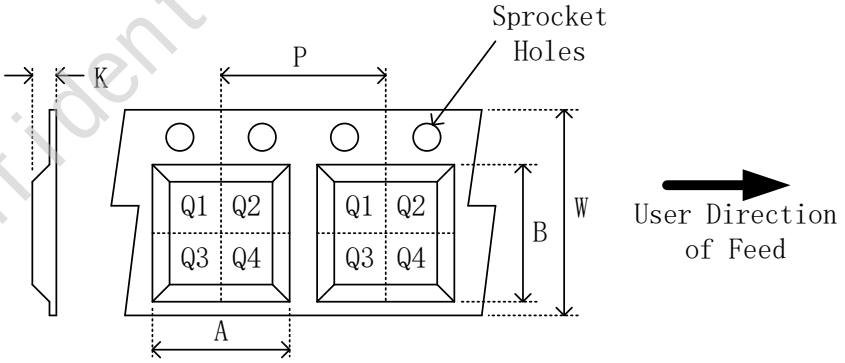


Figure 25. Reel Dimensions

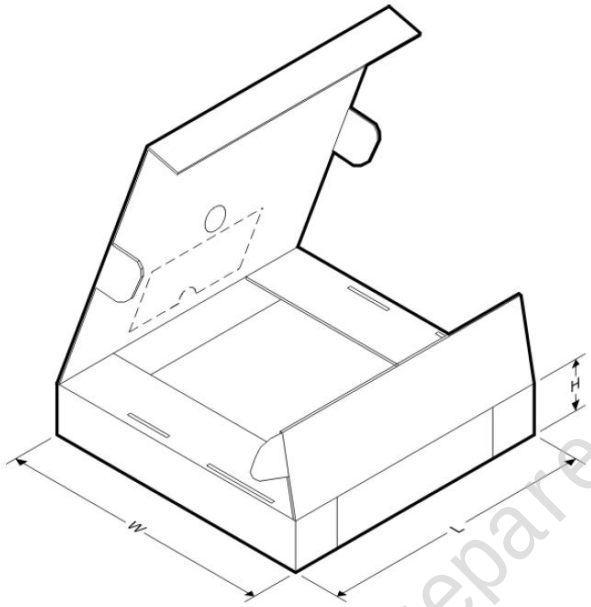


Device	Package Type	Pins	SPQ (pcs)	A (mm)	B (mm)	K (mm)	P (mm)	W (mm)	Pin1 Quadrant
MD18611GSA	SOT23-6	6	3000	3.23	3.17	1.37	4	8	Q3
MD18617GSC	SOT23-5	5	3000	3.23	3.17	1.37	4	8	Q3

Figure 26. Tape Dimensions and Quadrant Assignments for PIN 1 Orientation in Tape

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18. Tape and Reel Box Dimensions



Device	Package Type	Pins	SPQ (pcs)	Length (mm)	Width (mm)	Height (mm)
MD18611GSA	SOT23-6	6	30000	203	203	195
MD18617GSC	SOT23-5	5	30000	203	203	195

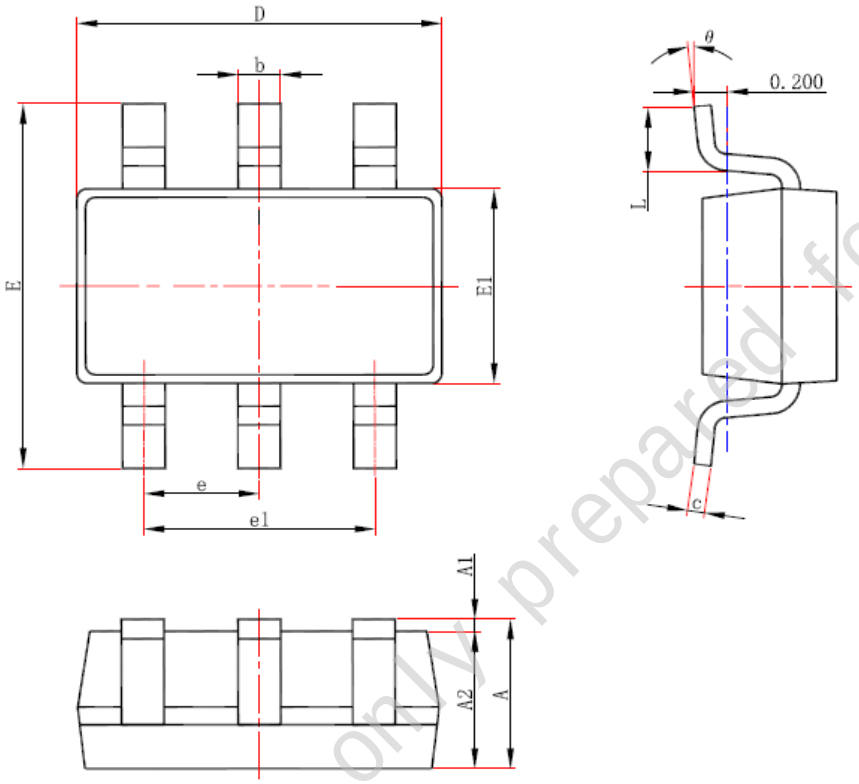
Figure 27. Box Dimensions

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19. Mechanical Data and Land Pattern Data

19.1 MD18611 Mechanical Data

SOT-23-6L（14R） PACKAGE OUTLINE DIMENSIONS



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	1.050	1.250	0.041	0.049
A1	0.000	0.100	0.000	0.004
A2	1.050	1.150	0.041	0.045
b	0.300	0.500	0.012	0.020
c	0.100	0.200	0.004	0.008
D	2.820	3.020	0.111	0.119
E1	1.500	1.700	0.059	0.067
E	2.650	2.950	0.104	0.116
e	0.950(BSC)		0.037(BSC)	
e1	1.800	2.000	0.071	0.079
L	0.300	0.600	0.012	0.024
θ	0°	8°	0°	8°

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19.2 MD18611 Land Pattern Data

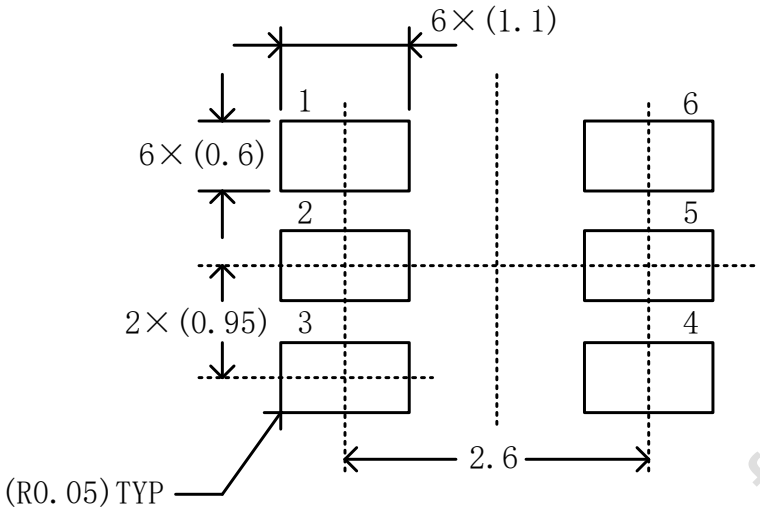


Figure 28. Land Pattern Example

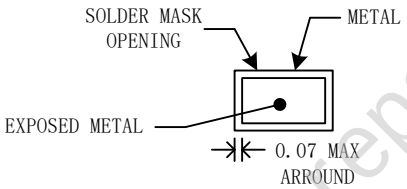
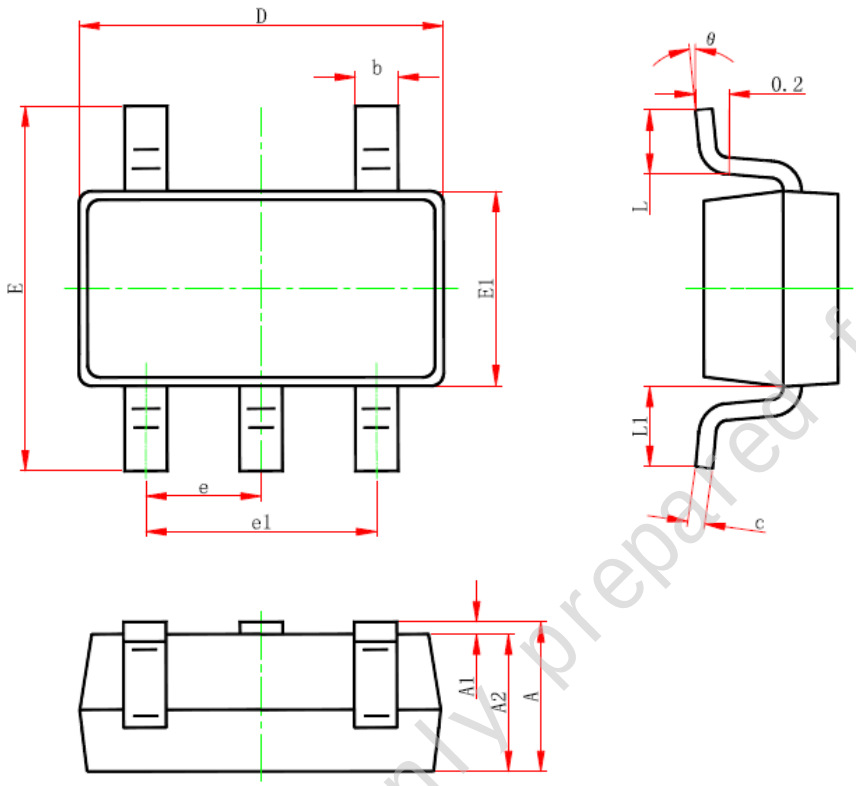


Figure 29. Non-Solder Mask Defined

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19.3 MD18617 Mechanical Data

SOT-23-5L(12R) PACKAGE OUTLINE DIMENSIONS



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	1.050	1.250	0.041	0.049
A1	0.000	0.100	0.000	0.004
A2	1.050	1.150	0.041	0.045
b	0.300	0.500	0.012	0.020
c	0.100	0.200	0.004	0.008
D	2.820	3.020	0.111	0.119
E1	1.500	1.700	0.059	0.067
E	2.650	2.950	0.104	0.116
e	0.950(BSC)		0.037(BSC)	
e1	1.800	2.000	0.071	0.079
L	0.300	0.600	0.012	0.024
L1	0.600REF.		0.024REF.	
θ	0°	8°	0°	8°

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19.4 MD18617 Land Pattern Data

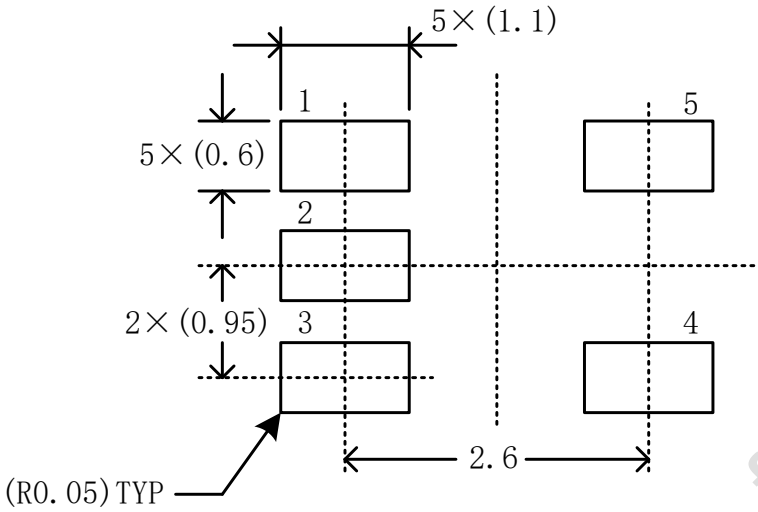


Figure 30. Land Pattern Example

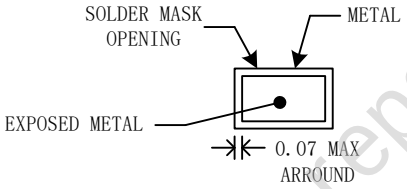


Figure 31. Non-Solder Mask Defined

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