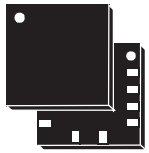
LSM303C

Ultra-compact high-performance eCompass module: 3D accelerometer and 3D magnetometer

Datasheet - production data



LGA-12 (2.0x2.0x1.0 mm)

Features

- 3 magnetic field channels and 3 acceleration channels
- ±16 gauss magnetic full scale
- ±2/±4/±8 *g* selectable acceleration full scale
- 16-bit data output
- SPI / I^2C serial interfaces
- Analog supply voltage 1.9 V to 3.6 V
- Power-down mode / low-power mode
- Programmable interrupt generators for free-fall, motion detection and magnetic field detection
- Embedded temperature sensor
- Embedded FIFO
- ECOPACK®, RoHS and “Green” compliant

Applications

- Tilt-compensated compasses
- Map rotation
- Position detection
- Motion-activated functions
- Free-fall detection
- Click/double-click recognition
- Pedometer
- Intelligent power saving for handheld devices
- Display orientation
- Gaming and virtual reality input devices
- Impact recognition and logging
- Vibration monitoring and compensation

Description

The LSM303C is a system-in-package featuring a 3D digital linear acceleration sensor and a 3D digital magnetic sensor.

The LSM303C has linear acceleration full scales of ±2 *g* / ±4 *g* / ±8 *g* and a magnetic field full scale of ±16 gauss.

The LSM303C includes an I^2C serial bus interface that supports standard and fast mode (100 kHz and 400 kHz) and an SPI serial standard interface.

The system can be configured to generate an interrupt signal for free-fall, motion detection and magnetic field detection.

The magnetic and accelerometer blocks can be enabled or put into power-down mode separately.

The LSM303C is available in a plastic land grid array package (LGA) and is guaranteed to operate over an extended temperature range from -40 °C to +85 °C.

Table 1. Device summary

Part number	Temperature range [°C]	Package	Packaging
LSM303C	-40 to +85	LGA-12	Tray
LSM303CTR	-40 to +85	LGA-12	Tape and reel

This is information on a product in full production. www.st.com

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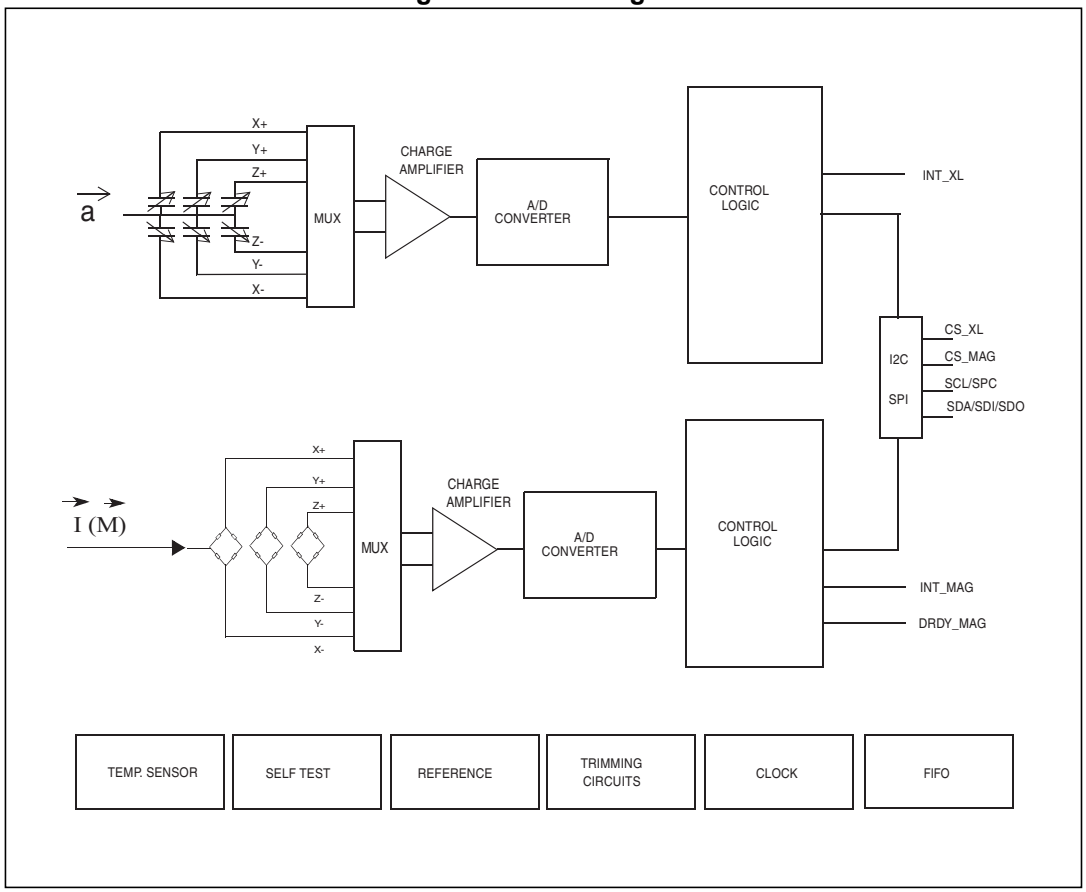
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1 Block diagram and pin description

1.1 Block diagram

Figure 1. Block diagram



1.2 Pin description

Figure 2. Pin connections

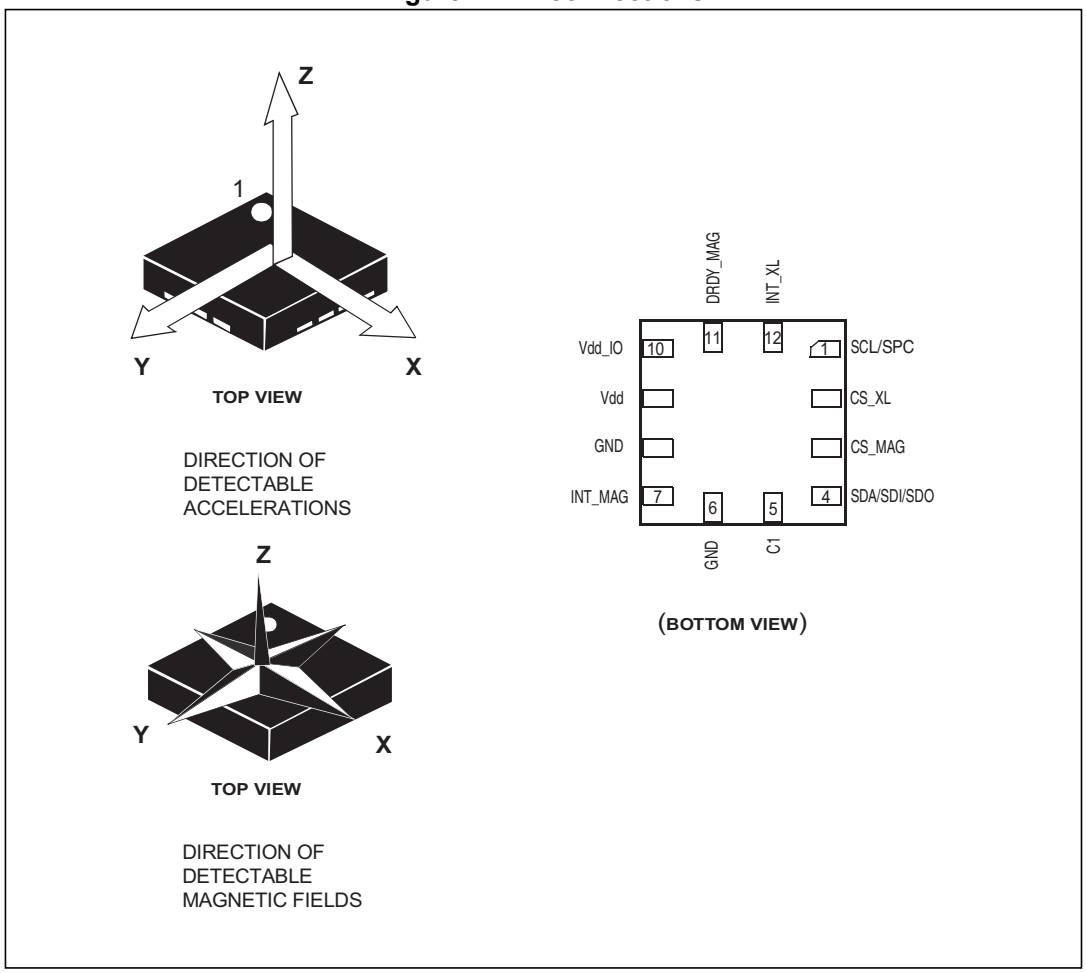


Table 2. Pin description

Pin#	Name	Function
1	SCL SPC	I^2C serial clock (SCL) SPI serial port clock (SPC)
2	CS_XL	Accelerometer: SPI enable I^2C/SPI mode selection 1: SPI idle mode / I^2C communication enabled; 0: SPI communication mode / I^2C disabled
3	CS_MAG	Magnetometer: SPI enable I^2C/SPI mode selection 1: SPI idle mode / I^2C communication enabled; 0: SPI communication mode / I^2C disabled
4	SDA SDI SDO	I^2C serial data (SDA) SPI serial data input (SDI) 3-wire interface serial data output (SDO)
5	C1	Capacitor connection (C1 = 100 nF)
6	GND	Connected to GND
7	INT_MAG	Magnetometer interrupt signal
8	GND	Connected to GND
9	Vdd	Power supply
10	Vdd_IO	Power supply for I/O pins
11	DRDY_MAG	Magnetometer data ready
12	INT_XL	Accelerometer interrupt signal

2 Module specifications

2.1 Sensor characteristics

@ Vdd = 2.5 V, T = 25 °C unless otherwise noted [a].

Table 3. Sensor characteristics

Symbol	Parameter	Test conditions	Min.	Typ.(1)	Max.	Unit
LA_FS	Linear acceleration measurement range(2)			±2		*g*
				±4		
				±8		
M_FS	Magnetic measurement range			±16		gauss
LA_So	Linear acceleration sensitivity	Linear acceleration FS = ±2 g		0.061		mg/LSB
		Linear acceleration FS = ±4 g		0.122		
		Linear acceleration FS = ±8 g		0.244		
M_GN	Magnetic sensitivity	Magnetic FS = ±16 gauss		0.58		mgauss/ LSB
LA_TCSo	Linear acceleration sensitivity change vs. temperature			0.01		%/°C
LA_TyOff	Typical zero-*g* level offset accuracy(3),(4)			±40		mg
M_TyOff	Typical zero-*gauss* level offset accuracy			±1		gauss
LA_TCOff	Zero-*g* level change vs. temp.	Max. delta from 25 °C		±0.5		mg/°C
LA_An	Linear acceleration RMS noise	ODR = 100 Hz, BW = 50 Hz, FS = ±2 *g*		1		mg (RMS)
M_R	Magnetic RMS noise	Ultra-high-performance mode		3.5		mgauss (RMS)
DF	Magnetic disturbance field	Zero-gauss offset starts to degrade			50	gauss
LA_ST	Linear acceleration self-test positive difference(5)		70		1500	mg
M_ST	Magnetic self-test(6)	X, Y-axis	-1		-3	gauss
		Z-axis	-0.1		-1	
Top	Operating temperature range		-40		+85	°C

1. Typical specifications are not guaranteed.
2. Verified by wafer level test and measurement of initial offset and sensitivity.
3. Typical zero-*g* level offset value after MSL3 preconditioning.
4. Offset can be eliminated by enabling the built-in high-pass filter.
5. Accelerometer “Self-test positive difference” is defined as: $OUTPUT[mg]_{(CTRL_REG5_A\ ST2,\ ST1\ bits=01)}$ - $OUTPUT[mg]_{(CTRL_REG5_A\ ST2,\ ST1\ bits=00)}$.
6. Magnetic “self-test” is defined as: $OUTPUT[gauss]_{(CTRL_REG1_M\ ST\ bit=1)}$ - $OUTPUT[gauss]_{(CTRL_REG1_M\ ST\ bit=0)}$.

a. The product is factory calibrated at 2.5 V. The operational power supply range is from 1.9 V to 3.6 V.

2.2 Temperature sensor characteristics

@ Vdd = 2.5 V, T = 25 °C unless otherwise noted[b].

Table 4. Temperature sensor characteristics

Symbol	Parameter	Test conditions	Min.	Typ.(1)	Max.	Unit
TSDr	Temperature sensor output change vs. temp.			8		digit/°C
TODR	Temperature refresh rate(2)			ODR		Hz
Top	Operating temperature range		-40		+85	°C

1. Typical specifications are not guaranteed.
2. If the TEMP_EN bit in *CTRL_REG1_M (20h)* is set to '1', temperature data is acquired at each conversion cycle. Refer to *Table 73: Output data rate configuration*

2.3 Electrical characteristics

@ Vdd = 2.5 V, T = 25 °C unless otherwise noted.[b]

Table 5. Electrical characteristics

Symbol	Parameter	Test conditions	Min.	Typ.(1)	Max.	Unit
Vdd	Supply voltage		1.9		3.6	V
Vdd_IO	Module power supply for I/O		1.71	1.8	Vdd+0.1	V
LA_Idd_NM	Linear acceleration current consumption in active mode. Magnetic sensor in power-down mode.	ODR = 100 - 800 Hz		180		µA
		ODR = 50 Hz		120		
		ODR =10 Hz		50		
M_Idd_HR	Magnetic current consumption in ultra-high resolution mode Linear acceleration in power-down mode.	ODR = 20 Hz		270		µA
M_Idd_LP	Magnetic current consumption in low-power mode Linear acceleration in power-down mode.	ODR = 20 Hz		40		µA
Idd_PD	Current consumption in power-down			6		µA
T_{OP}	Operating temperature range		-40		+85	°C
Trise	Time for power supply rising(2)		0.01		100	ms
Twait	Time delay between Vdd_IO and Vdd(2)		0		10	ms

1. Typical specifications are not guaranteed.
2. Please refer to *Section 2.3.1: Recommended power-up sequence* for more details.

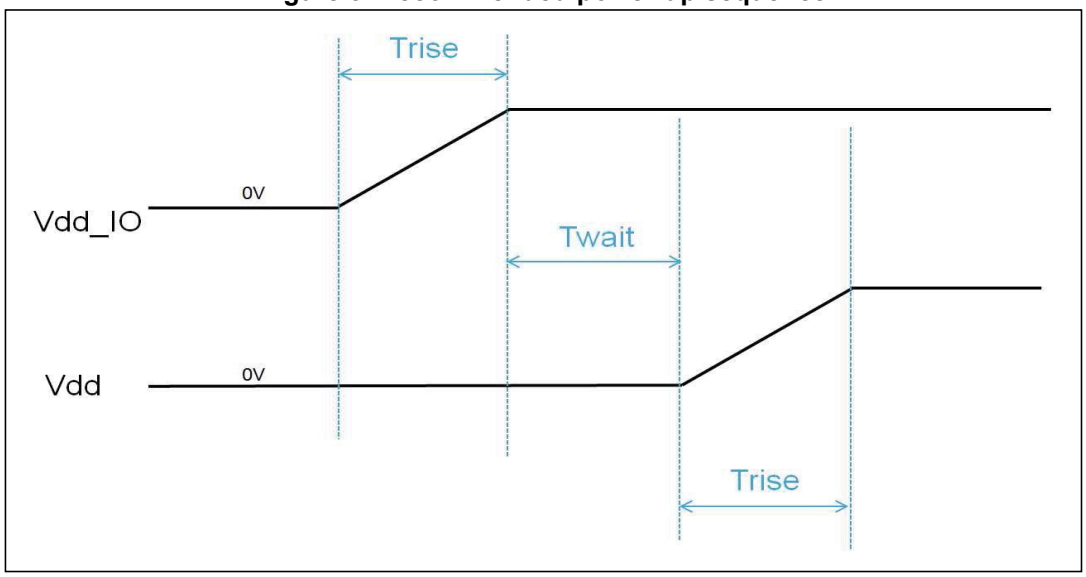
b. The product is factory calibrated at 2.5 V.The operational power supply range is from 1.9 V to 3.6 V.

2.3.1 Recommended power-up sequence

For the power-up sequence please refer to the following figure, where:

- Trise is the time for the power supply to rise from 10% to 90% of its final value
- Twait is the time delay between the end of the Vdd_IO ramp (90% of its final value) and the start of the Vdd ramp

Figure 3. Recommended power-up sequence



2.4 Communication interface characteristics

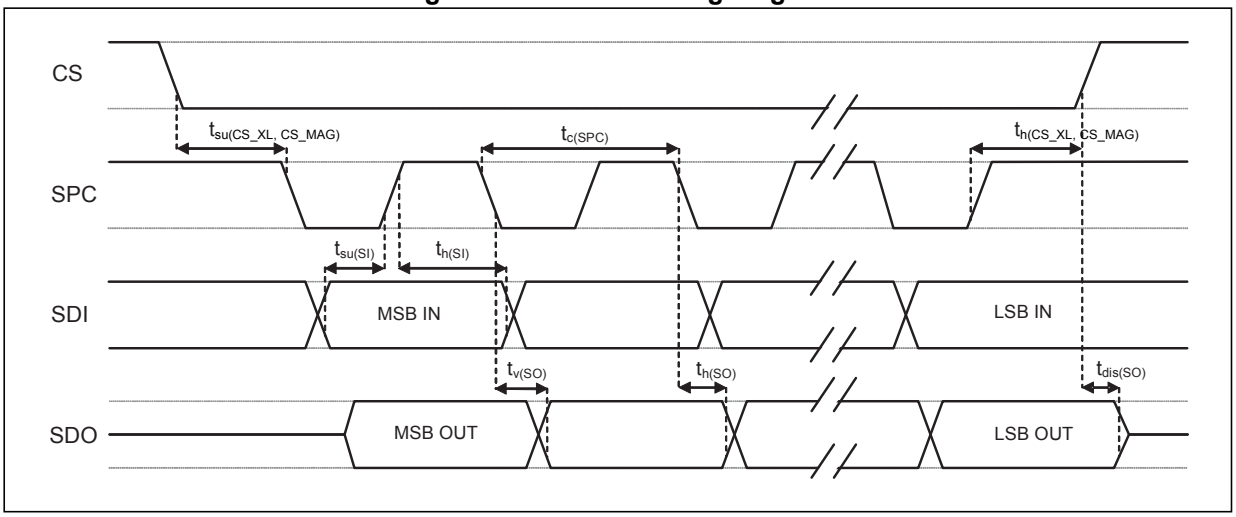
2.4.1 SPI - serial peripheral interface

Subject to general operating conditions for Vdd and Top.

Table 6. SPI slave timing values

Symbol	Parameter	Value (1)		Unit
		Min	Max	
$t_{c(SPC)}$	SPI clock cycle	100		ns
$f_{c(SPC)}$	SPI clock frequency		10	MHz
$t_{su(CS_XL,\ CS_MAG)}$	CS setup time	6		ns
$t_{h(CS_XL,\ CS_MAG)}$	CS hold time	8		
$t_{su(SI)}$	SDI input setup time	5		
$t_{h(SI)}$	SDI input hold time	15		
$t_{v(SO)}$	SDO valid output time		50	
$t_{h(SO)}$	SDO output hold time	9		
$t_{dis(SO)}$	SDO output disable time		50	

Figure 4. SPI slave timing diagram



Note: Values are guaranteed at 10 MHz clock frequency for SPI with 3 wires, based on characterization results, not tested in production.

Measurement points are done at 0.2·Vdd_IO and 0.8·Vdd_IO, for both input and output ports.

2.4.2 I²C - inter-IC control interface

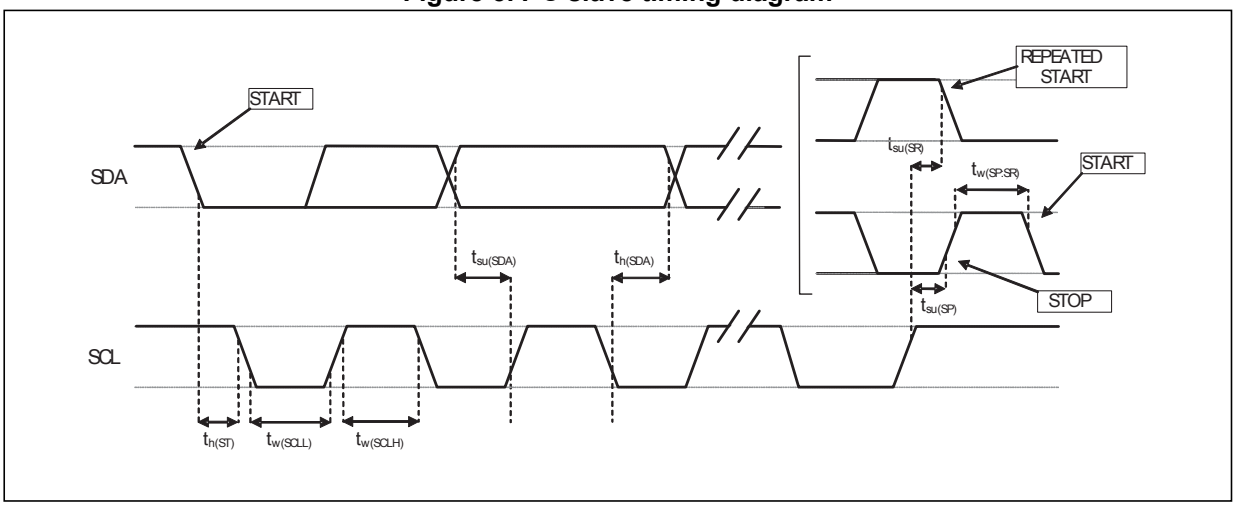
Subject to general operating conditions for Vdd and Top.

Table 7. I²C slave timing values

Symbol	Parameter	I²C standard mode (1)		I²C fast mode (1)		Unit
		Min	Max	Min	Max	
$f_{(SCL)}$	SCL clock frequency	0	100	0	400	kHz
$t_{w(SCLL)}$	SCL clock low time	4.7		1.3		µs
$t_{w(SCLH)}$	SCL clock high time	4.0		0.6		
$t_{su(SDA)}$	SDA setup time	250		100		ns
$t_{h(SDA)}$	SDA data hold time	0	3.45	0	0.9	µs
$t_{h(ST)}$	START condition hold time	4		0.6		µs
$t_{su(SR)}$	Repeated START condition setup time	4.7		0.6		
$t_{su(SP)}$	STOP condition setup time	4		0.6		
$t_{w(SP:SR)}$	Bus free time between STOP and START condition	4.7		1.3		

1. Data based on standard I²C protocol requirement, not tested in production

Figure 5. I²C slave timing diagram



Note: Measurement points are done at 0.2·Vdd_IO and 0.8·Vdd_IO, for both ports.

2.5 Absolute maximum ratings

Stresses above those listed as “absolute maximum ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 8. Absolute maximum ratings

Symbol	Ratings	Maximum value	Unit
Vdd	Supply voltage	-0.3 to 4.8	V
Vdd_IO	I/O pins supply voltage	-0.3 to 4.8	V
Vin	Input voltage on any control pin (CS_XL, CS_MAG, SCL/SPC, SDA/SDI/SDO)	-0.3 to Vdd_IO +0.3	V
A_{POW}	Acceleration (any axis, powered, Vdd = 2.5 V)	3000 for 0.5 ms	*g*
		10000 for 0.1 ms	*g*
A_{UNP}	Acceleration (any axis, unpowered)	3000 for 0.5 ms	*g*
		10000 for 0.1 ms	*g*
M_{EF}	Maximum exposed field	1000	gauss
T_{OP}	Operating temperature range	-40 to +85	°C
T_{STG}	Storage temperature range	-40 to +125	°C
ESD	Electrostatic discharge protection (HBM)	2	kV

Note: Supply voltage on any pin should never exceed 4.8 V

This device is sensitive to mechanical shock, improper handling can cause permanent damage to the part

This device is sensitive to electrostatic discharge (ESD), improper handling can cause permanent damage to the part

3 Terminology

3.1 Sensitivity

3.1.1 Linear acceleration sensor sensitivity

Sensitivity describes the gain of the sensor and can be determined by applying 1 *g* acceleration to it. As the sensor can measure DC accelerations this can be done easily by pointing the axis of interest towards the center of the Earth, noting the output value, rotating the sensor by 180 degrees (pointing to the sky) and noting the output value again. By doing so, ±1 *g* acceleration is applied to the sensor. Subtracting the larger output value from the smaller one, and dividing the result by 2, leads to the actual sensitivity of the sensor. This value changes very little over temperature and time. The sensitivity tolerance describes the range of sensitivities of a large population of sensors.

3.1.2 Magnetic sensor sensitivity

Sensitivity describes the gain of the sensor and can be determined, for example, by applying a magnetic field of 1 *gauss* to it.

3.2 Zero-*g* level

The zero-*g* level offset (LA_TyOff) describes the deviation of an actual output signal from the ideal output signal if no acceleration is present. A sensor in a steady state on a horizontal surface will measure 0 *g* for the X-axis and 0 *g* for the Y-axis whereas the Z-axis will measure 1 *g*. The output is ideally in the middle of the dynamic range of the sensor (content of OUT registers 00h, data expressed as two's complement number). A deviation from the ideal value in this case is called zero-*g* offset. Offset is to some extent a result of stress to MEMS sensor and therefore the offset can slightly change after mounting the sensor onto a printed circuit board or exposing it to extensive mechanical stress. Offset changes little with temperature, see *Table 3* "Zero-*g* level change vs. temperature" (LA_TCOff). The zero-*g* level tolerance (TyOff) describes the standard deviation of the range of zero-*g* levels of a population of sensors.

3.3 Zero-*gauss* level

Zero-*g*auss level offset (M_TyOff) describes the deviation of an actual output signal from the ideal output if no magnetic field is present.

4 Functionality

4.1 Self-test

The self-test allows checking the linear acceleration functionality without moving it. The self-test function is off when the self-test bits (ST) are programmed to ‘00’. When the self-test bits are changed, an actuation force is applied to the sensor, simulating a definite input acceleration. In this case the sensor outputs will exhibit a change in their DC levels which are related to the selected full scale through the device sensitivity. When the self-test is activated, the device output level is given by the algebraic sum of the signals produced by the acceleration acting on the sensor and by the electrostatic test force. If the output signals change within the amplitude limits specified inside *Table 3*, then the sensor is working properly and the parameters of the interface chip are within the defined specifications.

The self-test function is also available for the magnetic sensor. When the magnetic self-test is enabled, a current is forced into a coil near the sensor. This current will generate a magnetic field that will produce a variation of the magnetometer output signals. If the output signals change within the amplitude limits specified in *Table 3*, then the sensor is working properly and the parameters of the interface chip are within the defined specifications.

4.2 FIFO

The LSM303C embeds an acceleration data FIFO for each of the three output channels, X, Y and Z. This allows consistent power saving for the system, since the host processor does not need to continuously poll data from the sensor, but it can wake up only when needed and burst the significant data out from the FIFO. This buffer can work accordingly to the following different modes: Bypass mode, FIFO mode, Stream mode, Stream-to-FIFO mode, Bypass-to-Stream, Bypass-to-FIFO. Each mode is selected by the FIFO_MODE bits in the FIFO_CTRL register. Programmable FIFO threshold level, FIFO empty or FIFO overrun events are in the FIFO_SRC register and can be set to generate a dedicated interrupt on the INT_XL pin.

FIFO_SRC (EMPTY) is equal to '1' when no samples are available.

FIFO_SRC (FTH) goes to '1' if new data arrives and FIFO_SRC(FSS [4:0]) is greater than or equal to FIFO_CTRL (FTH [4:0]). FIFO_SRC (FTH) goes to '0' if reading a X, Y, Z data slot from FIFO and FIFO_SRC (FSS [4:0]) is less than or equal to FIFO_CTRL (FTH [4:0]).

FIFO_SRC (OVR) is equal to '1' if a FIFO slot is overwritten.

The FIFO feature is enabled by writing a '1' to the FIFO_EN bit in CTRL_REG3_A.

To guarantee the correct acquisition of data during the switching into and out of FIFO, the first sample acquired must be discarded.

4.2.1 Bypass mode

In Bypass mode (FIFO_CTRL (FMODE [2:0])= 000), the FIFO is not operational and it remains empty.

Bypass mode is also used to reset the FIFO when in FIFO mode.

4.2.2 FIFO mode

In FIFO mode (FIFO_CTRL (FMODE [2:0]) = 001) data from the X, Y and Z channels are stored in the FIFO until it is full. An overrun interrupt can be enabled, CTRL_REG3_A (INT_XL_OVR) = '1', in order to be raised when the FIFO stops collecting data. When the overrun interrupt occurs, the first set of data has been overwritten and the FIFO stops collecting data from the input channels. To reset the FIFO content, Bypass mode should be written in FIFO_CTRL (FMODE [2:0]) as '000'. After this reset command it is possible to restart FIFO mode by writing '001' to FIFO_CTRL (FMODE [2:0]).

The FIFO buffer can memorize 32 levels of X, Y and Z data, but the depth of the FIFO can be reduced by means of the CTRL_REG3_A (STOP_ FTH) bit. Setting the STOP_FTH bit to '1', the FIFO depth is limited to FIFO_CTRL (FTH [4:0]) - 1.

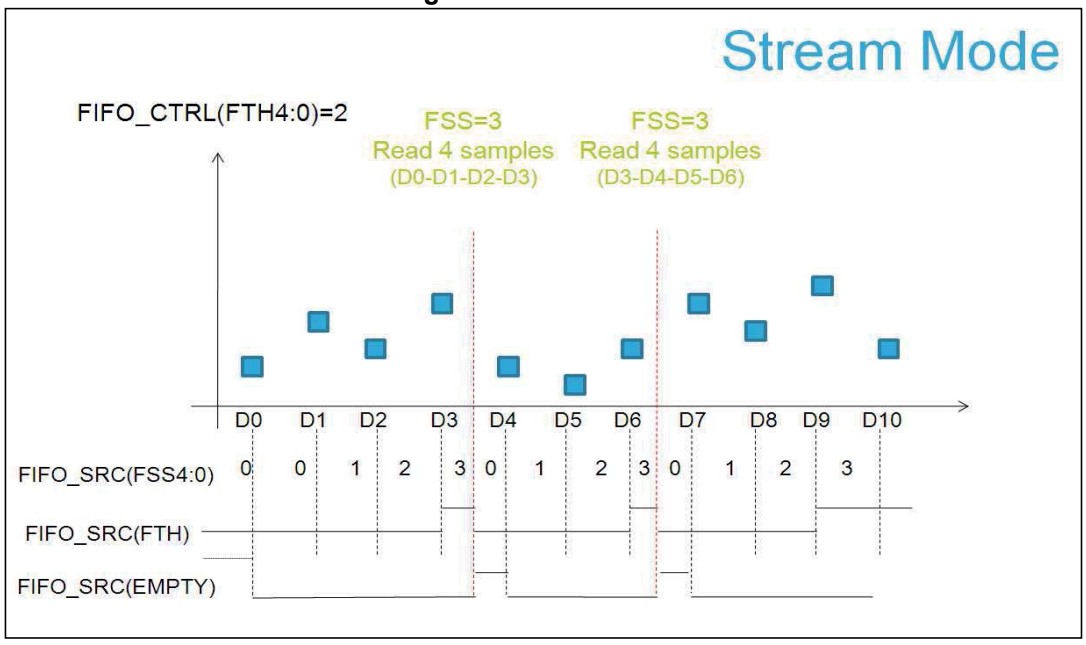
4.2.3 Stream mode

Stream mode (FIFO_CTRL (FMODE [2:0]) = 010) provides a continuous FIFO update. As new data arrives the older data is discarded.

An overrun interrupt can be enabled, CTRL_REG3_A (INT_XL_OVR) = '1', in order to read the entire content of the FIFO at once. If in the application no data can be lost and it is not possible to read at least one sample for each axis within one ODR period, a watermark interrupt can be enabled in order to read partially the FIFO and leave free memory slots for incoming data. Setting the FIFO_CTRL (FTH [4:0]) to an N value, the number of X, Y and Z data samples that should be read at the rise of the watermark interrupt is up to (N+1).

In the latter case, reading all FIFO content before an overrun interrupt has occurred, the first data read is equal to the last data already read in the previous burst, so the number of new data available in FIFO depends on the previous reading (see FIFO_SRC behavior depicted in the following figure).

Figure 6. Stream mode



Stream mode is intended to be used to read all 32 samples of FIFO within an ODR after receiving an overrun signal.

A watermark interrupt CTRL_REG3_A (INT_XL_FTH) can be enabled in order to read data from the FIFO and leave a free memory slot for incoming data. Setting the FIFO_CTRL (FTH [4:0]) to an N value, the number of X, Y and Z data samples that should be read at the rise of the watermark interrupt, in order to read the entire content of the FIFO, is N + 1.

4.2.4 Stream-to-FIFO mode

In Stream-to-FIFO mode (FIFO_CTRL(FMODE2:0) = 011), FIFO behavior changes according to the IG_SRC1_A (IA) bit. When the IG_SRC1_A(IA) bit is equal to '1', FIFO operates in FIFO mode, when the IG_SRC1_A (IA) bit is equal to '0', FIFO operates in Stream mode.

The interrupt generator 1 should be set to the desired configuration by means of IG_CFG1_A, IG_THS_X1_A, IG_THS_Y1_A and IG_THS_Z1_A.

The CTRL_REG7_A (LIR1) bit should be set to '1' in order to have latched interrupt.

4.2.5 Bypass-to-Stream mode

In Bypass-to-Stream mode (FIFO_CTRL (FMODE [2:0]) = '100'), X, Y and Z measurement storage inside FIFO operates in Stream mode when the IG_SRC1_A (IA) is equal to '1', otherwise FIFO content is reset (Bypass mode).

The interrupt generator 1 should be set to the desired configuration by means of IG_CFG1_A, IG_THS_X1_A, IG_THS_Y1_A and IG_THS_Z1_A.

The CTRL_REG7_A (LIR1) bit should be set to '1' in order to have latched interrupt.

4.2.6 Bypass-to-FIFO mode

In Bypass-to-FIFO mode (FIFO_CTRL (FMODE [2:0]) = '111', FIFO behavior changes according to the IG_SRC1_A(IA) bit. When the IG_SRC1_A(IA) bit is equal to '1,' FIFO operates in FIFO mode. When the IG_SRC1_A(IA) bit is equal to '0', FIFO operates in Bypass mode (FIFO content reset). If a latched interrupt is generated, FIFO starts collecting data until the first data into the FIFO buffer is overwritten. The interrupt generator 1 should be set to the desired configuration by means of IG_CFG1_A, IG_THS_X1_A, IG_THS_Y1_A and IG_THS_Z1_A.

The CTRL_REG7_A (LIR1) bit should be set to '1' in order to have latched interrupt.

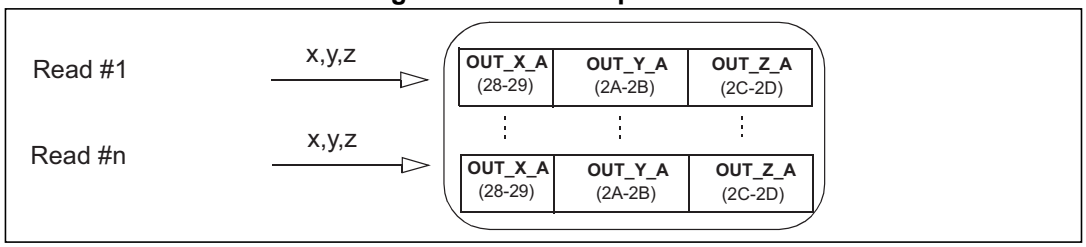
4.2.7 Retrieving data from FIFO

FIFO data is read from the OUT_X_A, OUT_Y_A and OUT_Z_A registers. A read operation using a serial interface of the OUT_X_A, OUT_Y_A or OUT_Z_A output registers provides the data stored in the FIFO. Each time data is read from the FIFO, the oldest X, Y and Z data are placed in the OUT_X_A, OUT_Y_A and OUT_Z_A registers and both single read and read_burst operations can be used.

4.2.8 FIFO multiple read (burst)

Starting from Addr 28h multiple reads can be performed. Once the read reaches Addr 2Dh the system automatically restarts from Addr 28h.

Figure 7. FIFO multiple read



4.3 Activity/Inactivity function

The Activity/Inactivity recognition function allows reducing the power consumption of the accelerometer block in order to supply other smart applications.

When the Activity/Inactivity recognition function is activated, accelerometer is able to automatically go to 10 Hz sampling rate and to wake up as soon as the interrupt event has been detected, increasing the output data rate and bandwidth.

With this feature the system may be efficiently switched from/to low-power mode to full performance depending on user-selectable positioning and acceleration events, thus ensuring power saving and flexibility.

The Activity/Inactivity recognition function is activated by writing the desired threshold in the ACT_THS_A register. The high-pass filter is automatically enabled.

Table 9. Activity/Inactivity function control registers

Register	LSB value
ACT_THS_A	Full Scale / 128 [mg]
ACT_DUR_A	8/ODR [s]

When the acceleration becomes smaller than the threshold for at least (8 ACT_DUR +1)/ODR time, the CTRL_REG1_A (ODR [2:0]) bits of CTRL_REG1_A are bypassed (Inactivity) and internally set to 10 Hz (ODR [2:0] = 001), but the content of the CTRL_REG1_A (ODR [2:0]) bits are left untouched.

When the acceleration becomes bigger than the threshold (ACT_THS_A), CTRL_REG1_A is restored immediately (Activity).

Once the Activity/Inactivity detection function is enabled, it will be applied to the INT_XL pin by setting the CTRL_REG3_A (INT_XL_INACT) bit to ‘1’.

To disable the Activity/Inactivity detection function, set the content of ACT_THS_A register to 00h.

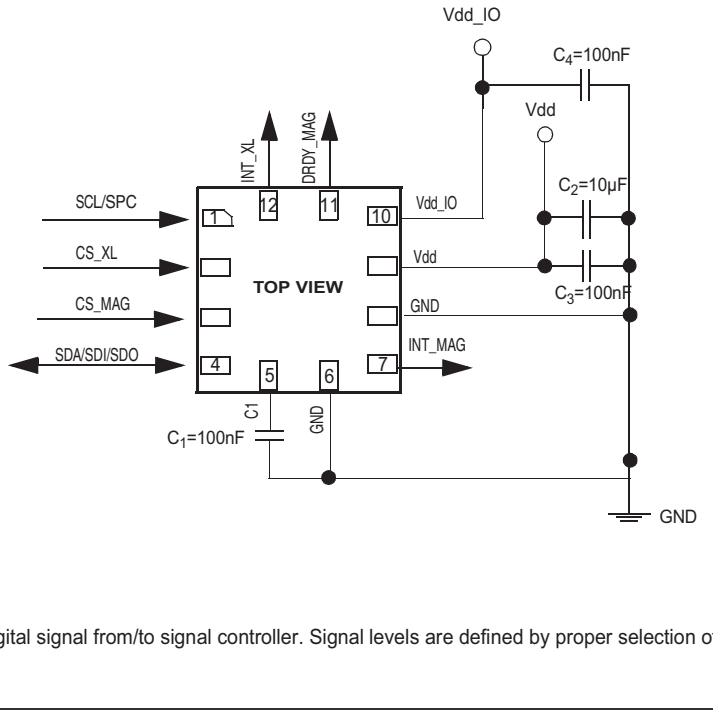
4.4 Factory calibration

The IC interface is factory calibrated for sensitivity (LA_So, M_GN), Zero-*g* level (LA_TyOff) and Zero-*gauss* level (M_TyOff).

The trim values are stored inside the device in non-volatile memory. Anytime the device is turned on, the trim parameters are downloaded into the registers to be used during active operation. This allows using the device without further calibration.

5 Application hints

Figure 8. LSM303C electrical connections



The device core is supplied through the Vdd line while the I/O pads are supplied through the Vdd_IO line. Power supply decoupling capacitors (100 nF ceramic, 10 µF aluminum) should be placed as near as possible to pin 9 of the device (common design practice).

All the voltage and ground supplies must be present at the same time to have proper behavior of the IC (refer to *Figure 8*). It is possible to remove Vdd, maintaining Vdd_IO, without blocking the communication bus, in this condition the measurement chain is powered off.

The functionality of the device and the measured acceleration data are selectable and accessible through the I^2C or SPI interfaces. When using the I^2C, CS must be tied high (i.e. connected to Vdd_IO).

The functions, the threshold and the timing of the two interrupt pins (INT_XL and INT_MAG) can be completely programmed by the user through the I^2C/SPI interface.

5.1 Soldering information

The LGA package is compliant with the ECOPACK®, RoHS and “Green” standards.
It is qualified for soldering heat resistance according to JEDEC J-STD-020.

Leave “Pin 1 Indicator” unconnected during soldering.

Land pattern and soldering recommendations are available at www.st.com.

5.2 High current wiring effects

High current in wiring and printed circuit traces can be culprits in causing errors in magnetic field measurements for compassing.

Conductor-generated magnetic fields will add to the Earth's magnetic field, leading to errors in compass heading computation.

Keep currents higher than 10 mA a few millimeters away from the sensor IC.

6 Digital interfaces

The registers embedded inside the LSM303C may be accessed through both the I^2C and SPI serial interfaces. The latter may be SW-configured to operate in 3-wire interface mode.

The serial interfaces are mapped onto the same pads. To select/exploit the I^2C interface, the CS line must be tied high (i.e. connected to Vdd_IO).

Table 10. Serial interface pin description

Pin name	Pin description
CS_XL, CS_MAG	SPI enable I2C/SPI mode selection (1: SPI idle mode / I^2C communication enabled; 0: SPI communication mode / I^2C disabled)
SCL SPC	I^2C serial clock (SCL) SPI serial port clock (SPC)
SDA SDI SDO	I^2C serial data (SDA) SPI serial data input (SDI) 3-wire interface serial data output (SDO)

6.1 I^2C serial interface

The LSM303C I^2C is a bus slave. The I^2C is employed to write data into registers whose content can also be read back.

The relevant I^2C terminology is given in the table below.

Table 11. Serial interface pin description

Term	Description
Transmitter	The device which sends data to the bus
Receiver	The device which receives data from the bus
Master	The device which initiates a transfer, generates clock signals and terminates a transfer
Slave	The device addressed by the master

There are two signals associated with the I^2C bus: the serial clock line (SCL) and the serial data line (SDA). The latter is a bidirectional line used for sending and receiving the data to/from the interface. Both the lines must be connected to Vdd_IO through an external pull-up resistor. When the bus is free, both the lines are high.

The I^2C interface is compliant with fast mode (400 kHz) I^2C standards as well as with the normal mode.

In order to disable the I^2C block for the accelerometer, CTRL_REG4_A (I2C_DISABLE) must be written to ‘1’, while for magnetometer CTRL_REG3_M (I2C_DISABLE) must be written to ‘1’.

6.1.1 I²C operation

The transaction on the bus is started through a START (ST) signal. A START condition is defined as a HIGH-to-LOW transition on the data line while the SCL line is held HIGH. After this has been transmitted by the master, the bus is considered busy. The next byte of data transmitted after the start condition contains the address of the slave in the first 7 bits and the eighth bit tells whether the master is receiving data from the slave or transmitting data to the slave. When an address is sent, each device in the system compares the first seven bits after a start condition with its address. If they match, the device considers itself addressed by the master.

Data transfer with acknowledge is mandatory. The transmitter must release the SDA line during the acknowledge pulse. The receiver must then pull the data line LOW so that it remains stable low during the HIGH period of the acknowledge clock pulse. A receiver which has been addressed is obliged to generate an acknowledge after each byte of data received.

The I²C embedded inside the LSM303C behaves like a slave device and the following protocol must be adhered to. In the I²C of the accelerometer sensor, after the START condition (ST) a slave address is sent, once a slave acknowledge (SAK) has been returned, an 8-bit sub-address (SUB) is transmitted. The 7 LSb represent the actual register address while the CTRL_REG4_A (IF_ADD_INC) bit defines the address increment. In the I²C of the magnetometer sensor, after the START condition (ST) a slave address is sent, once a slave acknowledge (SAK) has been returned, an 8-bit sub-address (SUB) is transmitted. The 7 LSb represent the actual register address while the MSB enables the address auto increment. The SUB (register address) is automatically increased to allow multiple data read/write.

Table 12. Transfer when master is writing one byte to slave

Master	ST	SAD + W		SUB		DATA		SP
Slave			SAK		SAK		SAK	

Table 13. Transfer when master is writing multiple bytes to slave

Master	ST	SAD + W		SUB		DATA		DATA		SP
Slave			SAK		SAK		SAK		SAK	

Table 14. Transfer when master is receiving (reading) one byte of data from slave

Master	ST	SAD + W		SUB		SR	SAD + R			NMAK	SP
Slave			SAK		SAK			SAK	DATA		

Table 15. Transfer when master is receiving (reading) multiple bytes of data from slave

Master	ST	SAD+W		SUB		SR	SAD+R			MAK		MAK		NMAK	SP
Slave			SAK		SAK			SAK	DATA		DAT A		DATA		

Data are transmitted in byte format (DATA). Each data transfer contains 8 bits. The number of bytes transferred per transfer is unlimited. Data is transferred with the Most Significant bit

(MSb) first. If a receiver can't receive another complete byte of data until it has performed some other function, it can hold the clock line SCL LOW to force the transmitter into a wait state. Data transfer only continues when the receiver is ready for another byte and releases the data line. If a slave receiver doesn't acknowledge the slave address (i.e. it is not able to receive because it is performing some real-time function) the data line must be left HIGH by the slave. The master can then abort the transfer. A LOW-to-HIGH transition on the SDA line while the SCL line is HIGH is defined as a STOP condition. Each data transfer must be terminated by the generation of a STOP (SP) condition.

In the presented communication format MAK is Master acknowledge and NMAK is No Master Acknowledge.

Default Address:

The accelerometer sensor slave address is 0011101b while magnetic sensor slave address is 0011110b.

The slave addresses are completed with a Read/Write bit. If the bit was '1' (Read), a repeated START (SR) condition must be issued after the two sub-address bytes. If the bit is '0' (Write) the master will transmit to the slave with direction unchanged. *Table 16* and *Table 17* explain how the SAD+Read/Write bit pattern are composed, listing all the possible configurations.

Linear acceleration sensor: the default (factory setting) 7-bit slave address is 0011101b.

Table 16. SAD + Read/Write patterns

Command	SAD[6:0]	R/W	SAD + R/W
Read	0011101	1	00111011 (3Bh)
Write	0011101	0	00111010 (3Ah)

Magnetic field sensor: the default (factory setting) 7-bit slave address is 0011110b.

Table 17. SAD + Read/Write patterns

Command	SAD[6:0]	R/W	SAD + R/W
Read	001110	1	00111101 (3Dh)
Write	001110	0	00111100 (3Ch)

6.2 SPI bus interface

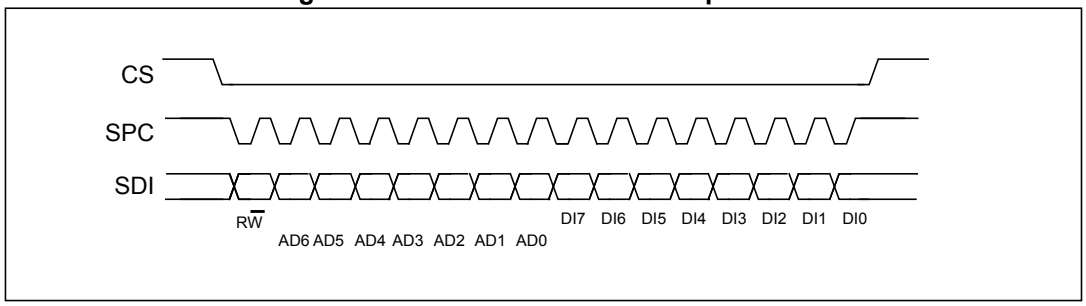
The LSM303C SPI is a bus slave. The SPI allows writing and reading the registers of the device.

The serial interface interacts with the outside world with 3 wires: **CS_XL**, **CS_MAG, SPC**, **SDI**.

3-wire mode is entered by setting the CTRL_REG4_A (SIM) and CTRL_REG3_M (SIM) bit equal to '1' (SPI serial interface mode selection).

6.2.1 Accelerometer SPI write

Figure 9. Accelerometer SPI write protocol



The SPI Write command is performed with 16 clock pulses. The multiple byte write command is performed by adding blocks of 8 clock pulses to the previous one.

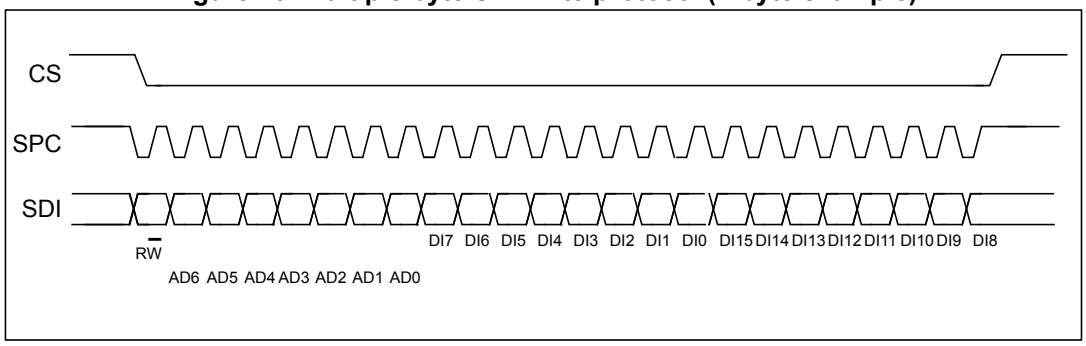
bit 0: WRITE bit. The value is 0.

bit 1 -7: address AD(6:0). This is the address field of the indexed register.

bit 8-15: data DI(7:0) (write mode). This is the data that is written inside the device (MSb first).

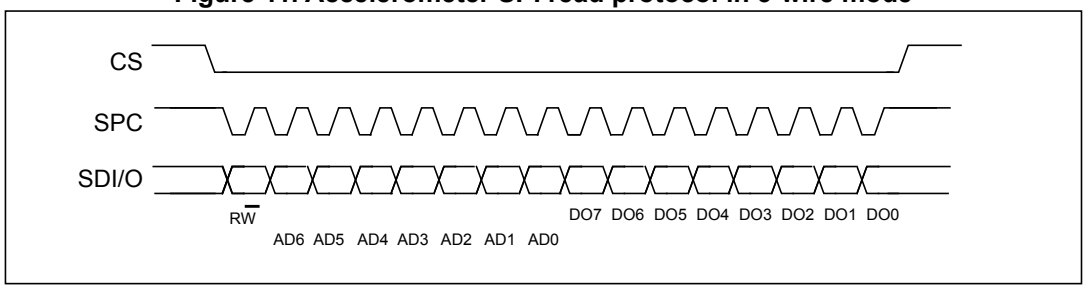
bit 16-... : data DI(...-8). Further data in multiple byte writes.

Figure 10. Multiple byte SPI write protocol (2-byte example)



6.2.2 Accelerometer SPI read in 3-wire mode

Figure 11. Accelerometer SPI read protocol in 3-wire mode



The SPI read command is performed with 16 clock pulses:

bit 0: READ bit. The value is 1.

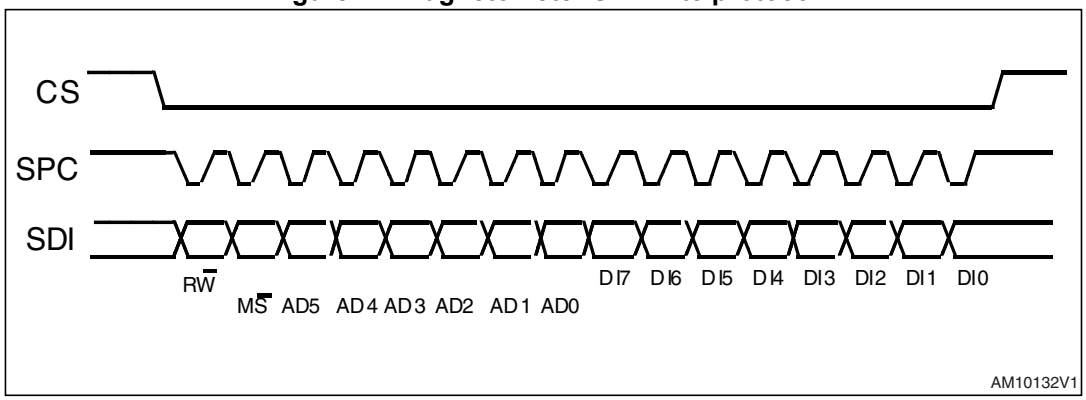
bit 1-7: address AD(6:0). This is the address field of the indexed register.

bit 8-15: data DO(7:0) (read mode). This is the data that is read from the device (MSb first).

The multiple read command is available in 3-wire mode.

6.2.3 Magnetometer SPI write

Figure 12. Magnetometer SPI write protocol



The SPI Write command is performed with 16 clock pulses. The multiple byte write command is performed by adding blocks of 8 clock pulses to the previous one.

bit 0: WRITE bit. The value is 0.

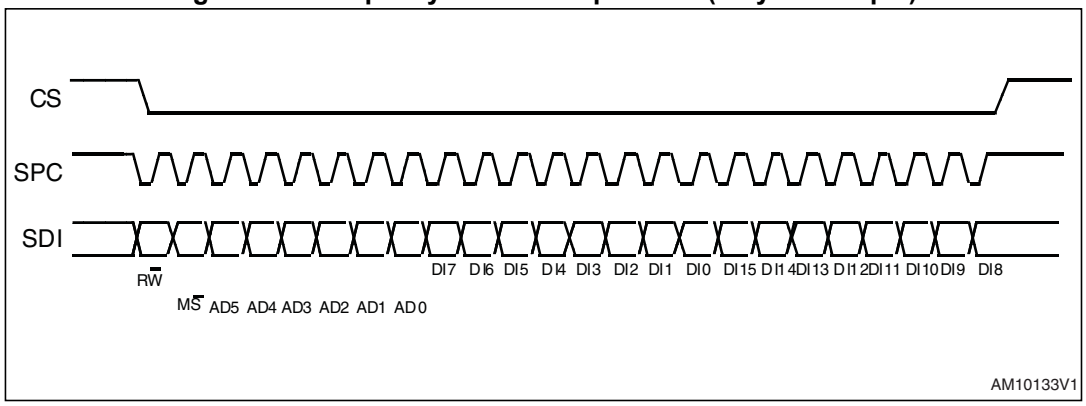
bit 1: MS bit. When 0 does not increment the address; when 1, increments the address in multiple writes.

bit 2 -7: address AD(5:0). This is the address field of the indexed register.

bit 8-15: data DI(7:0) (write mode). This is the data that is written inside the device (MSb first).

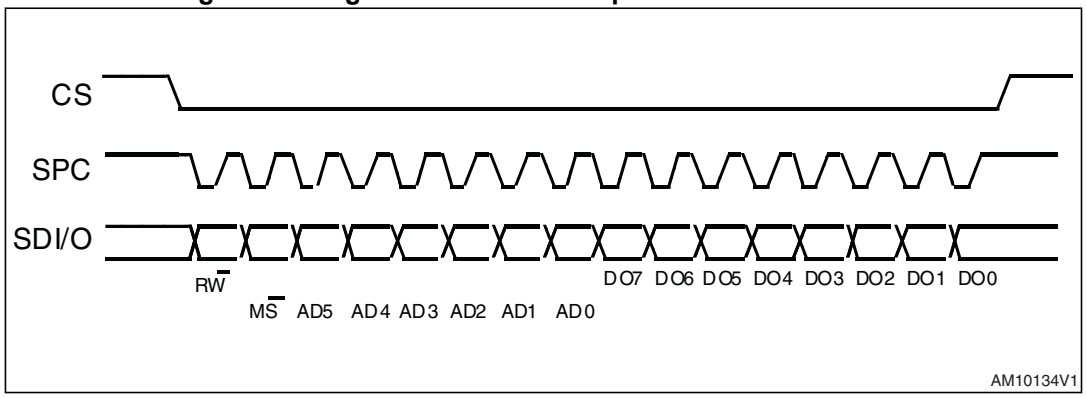
bit 16-... : data DI(...-8). Further data in multiple byte writes.

Figure 13. Multiple byte SPI write protocol (2-byte example)



6.2.4 Magnetometer SPI read

Figure 14. Magnetometer SPI read protocol in 3-wire mode



The SPI read command is performed with 16 clock pulses:

bit 0: READ bit. The value is 1.

bit 1: MS bit. When 0, does not increment the address; when 1, increments the address in multiple reads.

bit 2-7: address AD(5:0). This is the address field of the indexed register.

bit 8-15: data DO(7:0) (read mode). This is the data that is read from the device (MSb first).

The multiple read command is available in 3-wire mode.

7 Register mapping

The table given below provides a listing of the 8/16 bit registers embedded in the accelerometer and the corresponding address.

Table 18. Accelerometer register address map

Name	Type	Register address		Default	Comment
		Hex	Binary		
RESERVED	r	00-0E		-	Reserved
WHO_AM_I_A	r	OF	00001111	01000001	Accelerometer Who I am ID
ACT_THS_A	r/w	1E	00011110	00000000	
ACT_DUR_A	r/w	1F	00011111	00000000	
CTRL_REG1_A	r/w	20	00100000	00000111	Accelerometer control registers
CTRL_REG2_A	r/w	21	00100001	00000000	
CTRL_REG3_A	r/w	22	00100010	00000000	
CTRL_REG4_A	r/w	23	00100011	00000100	
CTRL_REG5_A	r/w	24	00100100	00000000	
CTRL_REG6_A	r/w	25	00100101	00000000	
CTRL_REG7_A	r/w	26	00100110	00000000	
STATUS_REG_A	r	27	00100111	output	Accelerometer status data register
OUT_X_L_A	r	28	00101000	output	Accelerometer output registers
OUT_X_H_A	r	29	00101001		
OUT_Y_L_A	r	2A	00101010		
OUT_Y_H_A	r	2B	00101011		
OUT_Z_L_A	r	2C	00101100		
OUT_Z_H_A	r	2D	00101101		
FIFO_CTRL	r/w	2E	00101110	00000000	Accelerometer FIFO registers
FIFO_SRC	r	2F	00101111	output	
IG_CFG1_A	r/w	30	00110000	00000000	Accelerometer interrupt generator 1 configuration
IG_SRC1_A	r	31	00110001	output	Accelerometer interrupt generator 1 status register
IG_THS_X1_A	r/w	32	00110010	00000000	Accelerometer interrupt generator 1 threshold X
IG_THS_Y1_A	r/w	33	00110011	00000000	Accelerometer interrupt generator 1 threshold Y
IG_THS_Z1_A	r/w	34	00110100	00000000	Accelerometer interrupt generator 1 threshold Z

Name	Type	Register address		Default	Comment
		Hex	Binary		
IG_DUR1_A	r/w	35	00110101	00000000	Accelerometer interrupt generator 1 duration
IG_CFG2_A	r/w	36	00110110	00000000	Accelerometer interrupt generator 2 configuration
IG_SRC2_A	r	37	00110111	output	Accelerometer interrupt generator 2 status register
IG_THS2_A	r/w	38	00111000	00000000	Accelerometer interrupt generator 2 threshold
IG_DUR2_A	r/w	39	00111001	00000000	Accelerometer interrupt generator 2 duration
XL_REFERENCE	r/w	3A	00111010	00000000	Reference X low
XH_REFERENCE	r/w	3B	00111011	00000000	Reference X high
YL_REFERENCE	r/w	3C	00111100	00000000	Reference Y low
YH_REFERENCE	r/w	3D	00111101	00000000	Reference Y high
ZL_REFERENCE	r/w	3E	00111110	00000000	Reference Z low
ZH_REFERENCE	r/w	3F	00111111	00000000	Reference Z high

Table 19. Magnetic sensor register address map:

Name	Type	Register address		Default	Comment
		Hex	Binary		
Reserved		00 - 0E	--	--	Reserved
WHO_AM_I_M	r	0F	0000 1111	00111101	Magnetic Who I am ID
Reserved		10 - 1F	--	--	Reserved
CTRL_REG1_M	r/w	20	0010 0000	00010000	Magnetic control registers
CTRL_REG2_M	r/w	21	0010 0001	00000000	
CTRL_REG3_M	r/w	22	0010 0010	00000011	
CTRL_REG4_M	r/w	23	0010 0011	00000000	
CTRL_REG5_M	r/w	24	0010 0100	00000000	
Reserved		25 - 26	--	--	Reserved
STATUS_REG_M	r	27	0010 0111	Output	
OUT_X_L_M	r	28	0010 1000	Output	Magnetic output registers
OUT_X_H_M	r	29	0010 1001	Output	
OUT_Y_L_M	r	2A	0010 1010	Output	
OUT_Y_H_M	r	2B	0010 1011	Output	
OUT_Z_L_M	r	2C	0010 1100	Output	
OUT_Z_H_M	r	2D	0010 1101	Output	

Name	Type	Register address		Default	Comment
		Hex	Binary		
TEMP_L_M	r	2E	0010 1110	Output	
TEMP_H_M	r	2F	0010 1111	Output	
INT_CFG_M	rw	30	00110000	00001000	Magnetic interrupt configuration register
INT_SRC_M	r	31	00110001	00000000	Magnetic interrupt generator status register
INT_THS_L_M	r	32	00110010	00000000	Magnetic interrupt generator threshold
INT_THS_H_M	r	33	00110011	00000000	

Registers marked as *Reserved* must not be changed. Writing to those registers may cause permanent damage to the device.

The content of the registers that are loaded at boot should not be changed. They contain the factory-calibrated values. Their content is automatically restored when the device is powered up.

8 Register description

8.1 WHO_AM_I_A (0Fh)

Accelerometer Who_AM_I register (r). This register is a read-only register. Its default value is 41h.

Table 20. WHO_AM_I_A register default value

0	1	0	0	0	0	0	1

8.2 ACT_THS_A (1Eh)

Activity threshold register (r/w). Its default value is 0x00. Inactivity threshold.

Table 21. ACT_THS_A register

-	THS6	THS5	THS4	THS3	THS2	THS1	THS0

8.3 ACT_DUR_A (1Fh)

Activity duration register (r/w). Its default value is 0x00. Activity duration.

Table 22. ACT_DUR_A register

DUR7	DUR6	DUR5	DUR4	DUR3	DUR2	DUR1	DUR0

8.4 CTRL_REG1_A (20h)

Accelerometer control register 1 (r/w)

Table 23. CTRL_REG1_A register

HR	ODR2	ODR1	ODR0	BDU	ZEN	YEN	XEN

Table 24. CTRL_REG1_A register description

HR	High-resolution bit. Default value: 0 0: normal mode, 1: high resolution (see *Table 26*)
ODR [2:0]	Output data rate & power mode selection. Default value: 000 (see *Table 25*)
BDU	Block Data Update. Default value:0 0: continuous update,1:output registers not updated until MSB and LSB read)
ZEN	Z-axis enable. Default value: 1 (0: Z-axis disabled; 1: Z-axis enabled)
YEN	Y-axis enable. Default value: 1 (0: Y-axis disabled; 1: Y-axis enabled)
XEN	X-axis enable. Default value: 1 (0: X-axis disabled; 1: X-axis enabled)

ODR [2:0] is used to set power mode and ODR selection. All frequencies available are given in the following table.

Table 25. ODR register setting

ODR2	ODR1	ODR0	ODR selection
0	0	0	Power down
0	0	1	10 Hz
0	1	0	50 Hz
0	1	1	100 Hz
1	0	0	200 Hz
1	0	1	400 Hz
1	1	0	800 Hz
1	1	1	N.A.

The BDU bit is used to inhibit the update of the output registers until both upper and lower register parts are read. In default mode (BDU = ‘0’) the output register values are updated continuously. When the BDU is activated (BDU = ‘1’), the content of the output registers is not updated until both MSB and LSB are read which avoids reading values related to different sample times.

Table 26. Low-pass cutoff frequency in high-resolution mode (HR = 1)

HR	CTRL_REG2_A (DFC [1:0])	LP cutoff freq. [Hz]
1	00	ODR/50
1	01	ODR/100
1	10	ODR/9
1	11	ODR/400

8.5 CTRL_REG2_A (21h)

Accelerometer control register 2 (r/w)

Table 27. CTRL_REG2_A register

-	DFC1	DFC0	HPM1	HPM0	FDS	HPIS2	HPIS1

Table 28. CTRL_REG2_A register description

DFC1 [1:0]	High-pass filter cutoff frequency selection: the bandwidth of the high-pass filter depends on the selected ODR and on the settings of the DFC [1:0] bits
HPM [1:0]	High-pass filter mode selection. Default value: 00 “00” or “10” = normal mode “01” = reference signal for filtering “11” = not available

FDS	High-pass filtered data selection. Default value: 0 (0: internal filter bypassed; 1: data from internal filter sent to output register and FIFO)
HPIS [2:1]	High Pass filter enabled for interrupt generator function on Interrupt 2 and Interrupt 1 (0: filter bypassed; 1: filter enabled)

8.6 CTRL_REG3_A (22h)

Accelerometer control register 3 (r/w). INT_XL control register

Table 29. CTRL_REG3_A register

FIFO_EN	STOP_FTH	INT_XL _INACT	INT_XL _IG2	INT_XL _IG1	INT_XL _OVR	INT_XL _FTH	INT_XL _DRDY

Table 30. CTRL_REG3_A register description

FIFO_EN	FIFO enable. Default value 0. (0: disable; 1: enable)
STOP_FTH	Enable FIFO threshold level use. Default value 0. (0: disable; 1: enable)
INT_XL_INACT	Inactivity interrupt on INT_XL. Default value 0. (0: disable; 1: enable)
INT_XL_IG2	Interrupt generator 2 on INT_XL. Default value 0. (0: disable; 1: enable)
INT_XL_IG1	Interrupt generator 1 on INT_XL. Default value 0. (0: disable; 1: enable)
INT_XL_OVR	FIFO overrun signal on INT_XL
INT_XL_FTH	FIFO threshold signal on INT_XL
INT_XL_DRDY	Data ready signal on INT_XL

8.7 CTRL_REG4_A (23h)

Accelerometer control register 4 (r/w)

Table 31. CTRL_REG4_A register

BW2	BW1	FS1	FS0	BW_SCALE_ODR	IF_ADD_INC	I2C_DISABLE	SIM

Table 32. CTRL_REG4_A register description

BW [2:1]	Anti aliasing filter bandwidth. Default value: 00 (00: 400 Hz; 01: 200 Hz; 10: 100 Hz; 11: 50 Hz)
FS [1:0]	Full-scale selection. Default value: 00 (00: ±2 *g*; 01: not available; 10: ±4 *g*; 11: ±8 *g*)

Table 32. CTRL_REG4_A register description

BW_SCALE _ODR	if '0' bandwidth is automatically selected according BW = 400 Hz when ODR = 800 Hz, 50 Hz, 10 Hz; BW = 200 Hz when ODR = 400 Hz; BW = 100 Hz when ODR = 200 Hz; BW = 50 Hz when ODR = 100 Hz; if '1' bandwidth is selected according to BW [2:1] excluding ODR = 50 Hz, 10 Hz, BW = 400 Hz
IF_ADD_INC	Register address automatically incremented during a multiple byte access with a serial interface (I^2C or SPI). (0: disable; 1: enable)
I2C_DISABLE	Disable I^2C interface. Default value 0. (0: I^2C enable; 1: I^2C disable)
SIM	SPI Serial Interface Mode selection. Default value: 0 0 = SPI write-only operations enabled; 1 = SPI read and write operations enabled

8.8 CTRL_REG5_A (24h)

Control register 5 (r/w)

Table 33. CTRL_REG5_A register

DEBUG	SOFT_RESET	DEC1	DEC0	ST2	ST1	H_LACTIVE	PP_OD

Table 34. CTRL_REG5_A register description

DEBUG	Debug stepping action selected. Default value: 0 (0: disable; 1: enable)
SOFT_RESET	Soft reset, it acts as POR when 1, then goes to 0
DEC [1:0]	Decimation of acceleration data on OUT REG and FIFO 00: no decimation 01: update every 2 samples 10: update every 4 samples 11: update every 8 samples
ST [2:1]	Self-test enable. Default value: 00 (00: self-test disabled; Other: see *Table 35*)
H_LACTIVE	Interrupt active high, low. Default value: 0 (0: active high; 1: active low)
PP_OD	Push-pull/open-drain selection on interrupt pad. Default value: 0 (0: push-pull; 1: open drain)

Table 35. Self-test mode selection

ST2	ST1	Self-test mode
0	0	Normal mode
0	1	Positive sign self-test
1	0	Negative sign self-test
1	1	Not allowed

8.9 CTRL_REG6_A (25h)

Accelerometer control register 6 (r/w)

Table 36. CTRL_REG6_A register

BOOT	-	-	-	-	-	-	-

Table 37. CTRL_REG6_A register description

BOOT	Force reboot, cleared as soon as the reboot is finished. Active high. Default value 0.

8.10 CTRL_REG7_A (26h)

Accelerometer control register 7 (r/w)

Table 38. CTRL_REG7_A register

-	-	DCRM2	DCRM1	LIR2	LIR1	4D_IG2	4D_IG1

Table 39. CTRL_REG7_A register description

DCRM [2:1]	DCRM is used to select the reset mode of the duration counter. Default value 0. If DCRM = '0', the counter is reset when the interrupt is no longer active, else if DCRM = '1', the duration counter is decremented. 1 LSB
LIR [2:1]	Latched Interrupt [2:1] Default value:0 (0: interrupt request not latched; 1: interrupt request latched) Cleared by reading IG_SRC[2:1]_A register
4D_IG [2:1]	Interrupt [2:1] 4D option enabled. Default value 0. When set, interrupt generator [2:1] uses 4D for position recognition.

8.11 STATUS_REG_A (27h)

Accelerometer status register (r/w)

Table 40. STATUS_REG_A register

ZYXOR	ZOR	YOR	XOR	ZYXDA	ZDA	YDA	XDA

Table 41. STATUS_REG_A register description

ZYXOR	X, Y and Z-axis data overrun. Default value: 0 (0: no overrun has occurred; 1: a new set of data has overwritten the previous data)
ZOR	Z-axis data overrun. Default value: 0 (0: no overrun has occurred; 1: a new set of data for the Z-axis has overwritten the previous data)

Table 41. STATUS_REG_A register description (continued)

YOR	Y-axis data overrun. Default value: 0 (0: no overrun has occurred; 1: new data for the Y-axis has overwritten the previous data)
XOR	X-axis data overrun. Default value: 0 (0: no overrun has occurred; 1: new data for the X-axis has overwritten the previous data)
ZYXDA	X, Y and Z-axis new data available. Default value: 0 (0: a new set of data is not yet available; 1: a new set of data is available)
ZDA	Z-axis new data available. Default value: 0 (0: new data for the Z-axis is not yet available; 1: new data for the Z-axis is available)
YDA	Y-axis new data available. Default value: 0 (0: new data for the Y-axis is not yet available; 1: new data for the Y-axis is available)
XDA	X axis new Data Available. Default value: 0 (0: new data for the X-axis is not yet available; 1: new data for the X-axis is available)

8.12 OUT_X_L_A (28h), OUT_X_H_A (29h)

Accelerometer x-axis output register (r)

Table 42. OUT_X_L_A register default values

0	0	0	0	0	0	0	0

Table 43. OUT_X_H_A register default values

0	0	0	0	0	0	0	0

8.13 OUT_Y_L_A (2Ah), OUT_Y_H_A (2Bh)

Accelerometer y-axis output register (r)

Table 44. OUT_Y_L_A register default values

0	0	0	0	0	0	0	0

Table 45. OUT_Y_H_A register default values

0	0	0	0	0	0	0	0

8.14 OUT_Z_L_A (2Ch), OUT_Z_H_A (2Dh)

Accelerometer z-axis output register (r)

Table 46. OUT_Z_L_A register default values

0	0	0	0	0	0	0	0

Table 47. OUT_Z_H_A register default values

0	0	0	0	0	0	0	0

8.15 FIFO_CTRL (2Eh)

FIFO control register (r/w)

Table 48. FIFO_CTRL register

FMODE2	FMODE1	FMODE0	FTH4	FTH3	FTH2	FTH1	FTH0

Table 49. FIFO_CTRL register description

FMODE [2:0]	FIFO mode selection bits. Default 000. For further details refer to *Table 50*
FTH [4:0]	FIFO threshold. Default: 00000. It is the FIFO depth if the STOP_FTH bit in the CTRL3 (22h) register is set to ‘1’.

Table 50. FIFO mode selection

FMODE2	FMODE1	FMODE0	Mode
0	0	0	Bypass mode. FIFO turned off
0	0	1	FIFO mode. Stops collecting data when FIFO is full.
0	1	0	Stream mode. If the FIFO is full, the new sample overwrites the older one
0	1	1	Stream mode until trigger is deasserted, then FIFO mode
1	0	0	Bypass mode until trigger is deasserted, then Stream mode
1	0	1	Not used
1	1	0	Not used
1	1	1	Bypass mode until trigger is deasserted, then FIFO mode

The FIFO trigger is the interrupt generator 1 event, all related information is available in *Section 8.18: IG_SRC1_A (31h)*.

8.16 FIFO_SRC (2Fh)

FIFO status control register (r)

Table 51. FIFO_SRC register

FTH	OVR	EMPTY	FSS4	FSS3	FSS2	FSS1	FSS0

Table 52. FIFO_SRC register description

FTH	FIFO threshold status. 0: FIFO filling is lower than FTH level; 1: FIFO filling is equal or higher than threshold level
OVR	Overrun bit status. 0: FIFO is not completely filled; 1: FIFO is completely filled
EMPTY	FIFO empty bit. 0: FIFO not empty; 1: FIFO empty)
FSS [4:0]	FIFO stored data level

8.17 IG_CFG1_A (30h)

Accelerometer interrupt generator 1 configuration register (r/w)

Table 53. IG_CFG1_A register

AOI	6D	ZHIE	ZLIE	YHIE	YLIE	XHIE	XLIE

Table 54. IG_CFG1_A register description

AOI	And/Or combination of Interrupt events. Default value: 0.
6D	6 direction detection function enabled. Default value: 0.
ZHIE	Enable interrupt generation on Z high event or on direction recognition. Default value: 0 (0: disable interrupt request; 1: enable interrupt request)
ZLIE	Enable interrupt generation on Z low event or on direction recognition. Default value: 0 (0: disable interrupt request; 1: enable interrupt request)
YHIE	Enable interrupt generation on Y low event or on direction recognition. Default value: 0 (0: disable interrupt request; 1: enable interrupt request)
YLIE	Enable interrupt generation on Y low event or on direction recognition. Default value: 0 (0: disable interrupt request; 1: enable interrupt request)
XHIE	Enable interrupt generation on X low event or on direction recognition. Default value: 0 (0: disable interrupt request; 1: enable interrupt request)
XLIE	Enable interrupt generation on X low event or on direction recognition. Default value: 0 (0: disable interrupt request; 1: enable interrupt request)

8.18 IG_SRC1_A (31h)

Accelerometer interrupt generator 1 status register (r)

Table 55. IG_SRC1_A register

-	IA	ZH	ZL	YH	YL	XH	XL

Table 56. IG_SRC1_A register description

IA	Interrupt active. Default value: 0 (0: no interrupt has been generated; 1: one or more interrupt events has been generated)
ZH	Z high. Default value: 0 (0: no interrupt; 1: ZH event has occurred)
ZL	Z low. Default value: 0 (0: no interrupt; 1: ZL event has occurred)
YH	Y high. Default value: 0 (0: no interrupt; 1: YH event has occurred)
YL	Y low. Default value: 0 (0: no interrupt; 1: YL event has occurred)
XH	X high. Default value: 0 (0: no interrupt; 1: XH event has occurred)
XL	X low. Default value: 0 (0: no interrupt; 1: XL event has occurred)

8.19 IG_THS_X1_A (32h), IG_THS_Y1_A (33h), IG_THS_Z1_A (34h)

Accelerometer interrupt generator 1 threshold registers (r/w)

Table 57. IG_THS register

THS7	THS6	THS5	THS4	THS3	THS2	THS1	THS0

Table 58. IG_THS register description

THS [7:0]	Interrupt 1 threshold. Default 00000000.

8.20 IG_DUR1_A (35h)

Accelerometer interrupt generator 1 duration register (r/w)

Table 59. IG_DUR1_A register

WAIT1	DUR1_6	DUR1_5	DUR1_4	DUR1_3	DUR1_2	DUR1_1	DUR1_0

Table 60. IG_DUR1_A register description

WAIT1	Wait function enable on duration counter. Default value: 0 (0: wait function off; 1: wait function on)
DUR1_[6:0]	Duration value. Default 0000000.

8.21 IG_CFG2_A (36h)

Accelerometer interrupt generator 2 configuration register (r/w)

Table 61. IG_CFG2_A register

AOI	6D	ZHIE	ZLIE	YHIE	YLIE	XHIE	XLIE

Table 62. IG_CFG2_A register description

AOI	And/Or combination of interrupt events. Default value: 0.
6D	6-direction detection function enabled. Default value: 0.
ZHIE	Enable interrupt generation on Z high event or on direction recognition. Default value: 0 (0: disable interrupt request; 1: enable interrupt request)
ZLIE	Enable interrupt generation on Z low event or on direction recognition. Default value: 0 (0: disable interrupt request; 1: enable interrupt request)
YHIE	Enable interrupt generation on Y low event or on direction recognition. Default value: 0 (0: disable interrupt request; 1: enable interrupt request)
YLIE	Enable interrupt generation on Y low event or on direction recognition. Default value: 0 (0: disable interrupt request; 1: enable interrupt request)
XHIE	Enable interrupt generation on Xlow event or on direction recognition. Default value: 0 (0: disable interrupt request;1: enable interrupt request)
XLIE	Enable interrupt generation on X low event or on direction recognition. Default value: 0 (0: disable interrupt request;1: enable interrupt request)

8.22 IG_SRC2_A (37h)

Accelerometer interrupt generator 2 status register (r)

Table 63. IG_SRC2_A register

-	IA	ZH	ZL	YH	YL	XH	XL

Table 64. IG_SRC2_A register description

IA	Interrupt active. Default value: 0 (0: no interrupt has been generated; 1: one or more interrupt events has been generated)
ZH	Z High. Default value: 0 (0: no interrupt; 1: ZH event has occurred)
ZL	Z Low. Default value: 0 (0: no interrupt; 1: ZL event has occurred)
YH	Y High. Default value: 0 (0: no interrupt; 1: YH event has occurred)
YL	Y Low. Default value: 0 (0: no interrupt; 1: YL event has occurred)
XH	X High. Default value: 0 (0: no interrupt; 1: XH event has occurred)
XL	X Low. Default value: 0 (0: no interrupt; 1: XL event has occurred)

8.23 IG_THS2_A (38h)

Accelerometer interrupt generator 2 threshold register (r/w)

Table 65. IG_THS2_A register

THS7	THS6	THS5	THS4	THS3	THS2	THS1	THS0

Table 66. IG_THS2_A register description

THS [7:0]	Interrupt generator 2 threshold. Default 00000000.

8.24 IG_DUR2_A (39h)

Accelerometer interrupt generator 2 duration register (r/w)

Table 67. IG_DUR2_A register

WAIT2	DUR2_6	DUR2_5	DUR2_4	DUR2_3	DUR2_2	DUR2_1	DUR2_0

Table 68. IG_DUR2_A register description

WAIT2	Wait function enable on duration counter. Default value: 0 (0: wait function off; 1: wait function on)
DUR2_[6:0]	Duration value. Default 0000000.

8.25 XL_REFERENCE (3Ah), XH_REFERENCE (3Bh)

In normal mode (HPM [1:0] = ‘00’ or ‘10’) when one of these registers (XL_REFERENCE or XH_REFERENCE) is read, the X output of the hp filter is set to ‘0’. In reference mode (HPM [1:0] =”01”) the reference value is subtracted from the X output of the hp filter.

8.26 YL_REFERENCE (3Ch), YH_REFERENCE (3Dh)

See above comment for X Reference (r/w).

8.27 ZL_REFERENCE (3Eh), ZH_REFERENCE (3Fh)

See above comment for X Reference (r/w).

8.28 WHO_AM_I_M (0Fh)

Device identification register.

Table 69. WHO_AM_I_M register

0	0	1	1	1	1	0	1

8.29 CTRL_REG1_M (20h)

Table 70. CTRL_REG1_M register

TEMP_EN	OM1	OM0	DO2	DO1	DO0	0(1)	ST

1. This bit must be set to ‘0’ for the correct operation of the device

Table 71. CTRL_REG1_M register description

TEMP_EN	Temperature sensor enable. Default value: 0 (0: temperature sensor disabled; 1: temperature sensor enabled)
OM[1:0]	X and Y axes operative mode selection. Default value: 00 (Refer to *Table 72*)
DO[2:0]	Output data rate selection. Default value: 100 (Refer to *Table 73*)
ST	Self-test enable. Default value: 0 (0: self-test disabled; 1: self-test enabled)

Table 72. X and Y axes operative mode selection

OM1	OM0	Operative mode for X and Y axes
0	0	Low-power mode
0	1	Medium-performance mode
1	0	High-performance mode
1	1	Ultra-high performance mode

Table 73. Output data rate configuration

DO2	DO1	DO0	ODR [Hz]
0	0	0	0.625
0	0	1	1.25
0	1	0	2.5
0	1	1	5
1	0	0	10
1	0	1	20
1	1	0	40
1	1	1	80

8.30 CTRL_REG2_M (21h)

Table 74. CTRL_REG2_M register

0(1)	FS1	FS0	0(1)	REBOOT	SOFT_RST	0(1)	0(1)

1. These bits must be set to ‘0’ for the correct operation of the device

Table 75. CTRL_REG2_M register description

FS[1:0]	Full-scale configuration. Default value: 00 Refer to *Table 76*
REBOOT	Reboot memory content. Default value: 0 (0: normal mode; 1: reboot memory content)
SOFT_RST	Configuration registers and user register reset function. (0: default value; 1: reset operation)

Table 76. Full-scale selection

FS1	FS0	Full scale
0	0	Not used
0	1	Not used
1	0	Not used
1	1	± 16 gauss

8.31 CTRL_REG3_M (22h)

Table 77. CTRL_REG3_M register

I2C_DISABLE	0(1))	LP	0(1)	0(1)	SIM	MD1	MD0

1. These bits must be set to ‘0’ for the correct operation of the device.

Table 78. CTRL_REG3_M register description

I2C_DISABLE	Disable I^2C interface. Default value 0. (0: I^2C enable; 1: I^2C disable)
LP	Low-power mode configuration. Default value: 0 If this bit is '1', the DO[2:0] is set to 0.625 Hz and the system performs, for each channel, the minimum number of averages. Once the bit is set to '0', the magnetic data rate is configured by the DO bits in *CTRL_REG1_M (20h)* register.
SIM	SPI Serial Interface mode selection. Default value: 0 (0= SPI only write operations enabled; 1= SPI read and write operations enable).
MD[1:0]	Operating mode selection. Default value: 11 Refer to *Table 79.*

Table 79. System operating mode selection

MD1	MD0	Mode
0	0	Continuous-conversion mode
0	1	Single-conversion mode Single-conversion mode has to be used with sampling frequency from 0.625 Hz to 80 Hz.
1	0	Power-down mode
1	1	Power-down mode

8.32 CTRL_REG4_M (23h)

Table 80. CTRL_REG4_M register

0(1)	0(1)	0(1)	0(1)	OMZ1	OMZ0	BLE	0(1)

1. These bits must be set to '0' for the correct operation of the device

Table 81. CTRL_REG4_M register description

OMZ[1:0]	Z-axis operative mode selection. Default value: 00. Refer to *Table 82.*
BLE	Big/Little Endian data selection. Default value: 0 (0: data LSb at lower address; 1: data MSb at lower address)

Table 82. Z-axis operative mode selection

OMZ1	OMZ0	Operative mode for Z-axis
0	0	Low-power mode
0	1	Medium-performance mode
1	0	High-performance mode
1	1	Ultra-high performance mode

8.33 CTRL_REG5_M (24h)

Table 83. CTRL_REG5_M register

0(1)	BDU	0(1)	0(1)	0(1)	0(1)	0(1)	0(1)

1. These bits must be set to '0' for the correct operation of the device.

Table 84. CTRL_REG5_M register description

BDU	Block data update for magnetic data. Default value: 0 (0: continuous update; 1: output registers not updated until MSB and LSB have been read)

8.34 STATUS_REG_M (27h)

Table 85. STATUS_REG_M register

ZYXOR	ZOR	YOR	XOR	ZYXDA	ZDA	YDA	XDA

Table 86. STATUS_REG_M register description

ZYXOR	X, Y and Z-axis data overrun. Default value: 0 (0: no overrun has occurred; 1: a new set of data has overwritten the previous data)
ZOR	Z-axis data overrun. Default value: 0 (0: no overrun has occurred; 1: new data for the Z-axis has overwritten the previous data)
YOR	Y-axis data overrun. Default value: 0 (0: no overrun has occurred; 1: new data for the Y-axis has overwritten the previous data)
XOR	X-axis data overrun. Default value: 0 (0: no overrun has occurred; 1: new data for the X-axis has overwritten the previous data)
ZYXDA	X, Y and Z-axis new data available. Default value: 0 (0: a new set of data is not yet available; 1: a new set of data is available)
ZDA	Z-axis new data available. Default value: 0 (0: new data for the Z-axis is not yet available; 1: new data for the Z-axis is available)
YDA	Y-axis new data available. Default value: 0 (0: new data for the Y-axis is not yet available; 1: new data for the Y-axis is available)
XDA	X-axis new data available. Default value: 0 (0: a new data for the X-axis is not yet available; 1: a new data for the X-axis is available)

8.35 OUT_X_L_M (28h), OUT_X_H_M(29h)

Magnetometer X-axis data output. The value of the magnetic field is expressed as two's complement.

8.36 OUT_Y_L_M (2Ah), OUT_Y_H_M (2Bh)

Magnetometer Y-axis data output. The value of the magnetic field is expressed as two's complement.

8.37 OUT_Z_L_M (2Ch), OUT_Z_H_M (2Dh)

Magnetometer Z-axis data output. The value of the magnetic field is expressed as two's complement.

8.38 TEMP_L_M(2Eh), TEMP_H_M (2Fh)

Temperature sensor data. The value of the temperature is expressed as two's complement.

8.39 INT_CFG_M (30h)

Table 87. INT_CFG_M register

XIEN	YIEN	ZIEN	0(1)	1(2)	IEA	IEL	IEN

1. This bit must be set to '0' for the correct operation of the device.
2. This bit must be set to '1' for the correct operation of the device.

Table 88. INT_CFG_M register description

XIEN	Enable interrupt generation on X-axis. Default value: 0 0: disable interrupt request; 1: enable interrupt request
YIEN	Enable interrupt generation on Y-axis. Default value: 0 0: disable interrupt request; 1: enable interrupt request
ZIEN	Enable interrupt generation on Z-axis. Default value: 0 0: disable interrupt request; 1: enable interrupt request
IEA	Interrupt active configuration on INT_MAG. Default value: 0 0: low; 1: high
IEL	Latch interrupt request. Default value: 0 0: interrupt request latched; 1: interrupt request not latched) Once latched, the INT_MAG pin remains in the same state until *INT_SRC_M (31h)*) is read.
IEN	Interrupt enable on the INT_MAG pin. Default value: 0 0: disable; 1: enable

8.40 INT_SRC_M (31h)

Table 89. INT_SRC_M register

PTH_X	PTH_Y	PTH_Z	NTH_X	NTH_Y	NTH_Z	MROI(1)	INT

1. This functionality can be enabled only if the IEN bit in *INT_CFG_M (30h)* is enabled.

Table 90. INT_SRC_M register description

PTH_X	Value on X-axis exceeds the threshold on the positive side. Default value: 0.
PTH_Y	Value on Y-axis exceeds the threshold on the positive side. Default value: 0.
PTH_Z	Value on Z-axis exceeds the threshold on the positive side. Default value: 0.
NTH_X	Value on X-axis exceeds the threshold on the negative side. Default value: 0.
NTH_Y	Value on Y-axis exceeds the threshold on the negative side. Default value: 0.
NTH_Z	Value on Z-axis exceeds the threshold on the negative side. Default value: 0.
MROI	Internal measurement range overflow on magnetic value. Default value: 0.
INT	This bit signals when the interrupt event occurs.

8.41 INT_THS_L_M (32h), INT_THS_H_M (33h)

Interrupt threshold. Default value: 0.

The value is expressed in 15-bit unsigned.

Even if the threshold is expressed in absolute value, the device detects both positive and negative thresholds.

Table 91. INT_THS_L_M register

THS7	THS6	THS5	THS4	THS3	THS2	THS1	THS0

Table 92. INT_THS_H_M register

0(1)	THS14	THS13	THS12	THS11	THS10	THS9	THS8

1. This bit must be set to ‘0’ for the correct operation of the device.

9 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

Table 93. LGA-12 2x2x1 mm mechanical dimensions (see note 1 and 2)

Databook				
Symbol	**Min.**	**Typ.**	**Max.**	**Note**
Θ	-	45°	-	
A	-	-	1.00	
A1	0.00	-	0.05	4
A2	-	0.13	-	
b	-	0.25	-	7
D		2.00		6
E		2.00		6
e		0.50		
e1		1.50		
h	-	0.075	-	
L	-	0.275	-	7
L1	-	0.10	-	
N		12		5

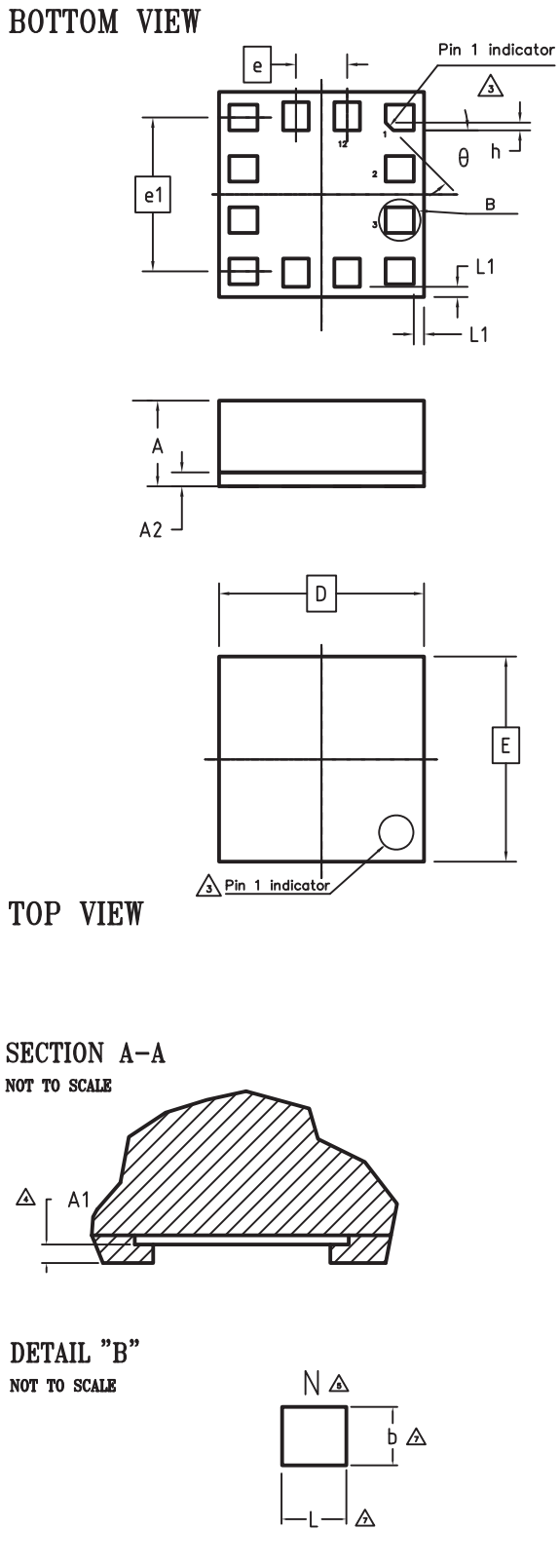
Symbol	**Tolerance of Form and Position**
	Databook
D/E	0.15
Notes	1 and 2
REF	-

Δ

Note:

1. *Dimensioning and tolerancing schemes conform to ASME Y14.5M-1994.*
2. *All dimensions are in millimeters.*
3. *The "Pin 1 Indicator" is identified on top and/or bottom surfaces of the package.*
4. *A1 is defined as the distance from the seating plane to the land.*
5. *"N" is the maximum number of terminal positions for the specified body size.*
6. *The tolerance of the typical value is specified in the table "Tolerance of Form and Position".*
7. *Dimensions "b" and "L" are specified:*
   For solder mask defined: at terminal plating surface
   For non-solder mask defined: at solder mask opening

Figure 15. LGA-12 2x2x1 mm mechanical drawing



10 Revision history

Table 94. Document revision history

Date	Revision	Changes
12-Jul-2013	1	Initial release
13-Jun-2014	2	Document status promoted from preliminary data to production data Added Trise and Twait to *Table 5: Electrical characteristics* Added *Section 2.3.1: Recommended power-up sequence*

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