CSD97376Q4M 同步降压 NexFET™ 功率级

Not Recommended for New Designs

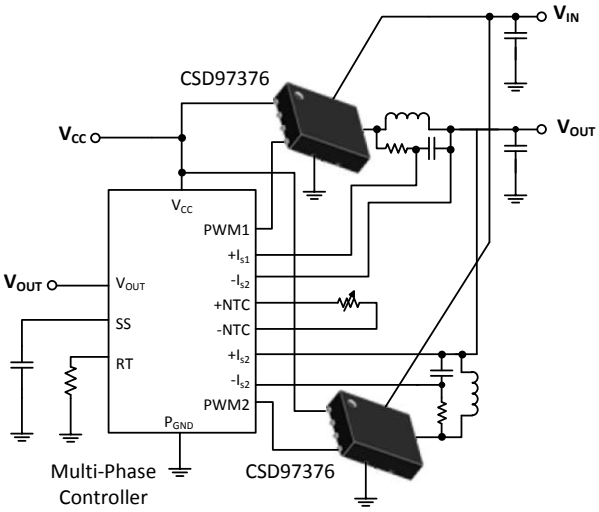
1 特性

- 在 15A 的电流下具有 90% 的系统效率
- 最大额定持续电流 20A，峰值电流 45A
- 高频运行（高达 2MHz）
- 高密度 3.5mm x 4.5mm SON 封装
- 超低电感封装
- 系统已优化的印刷电路板 (PCB) 封装
- 超低静态 (ULQ) 电流模式
- 兼容 3.3V 和 5V PWM 信号
- 支持 FCCM 的二极管仿真模式
- 输入电压高达 24V
- 三态 PWM 输入
- 集成型自举二极管
- 击穿保护
- 符合 RoHS 环保标准 – 无铅引脚镀层
- 无卤素

2 应用

- 超级本/笔记本 DC/DC 转换器
- 多相 Vcore 和 DDR 解决方案
- 在网络互联、电信、和计算系统中的负载点同步降压

应用图表



3 说明

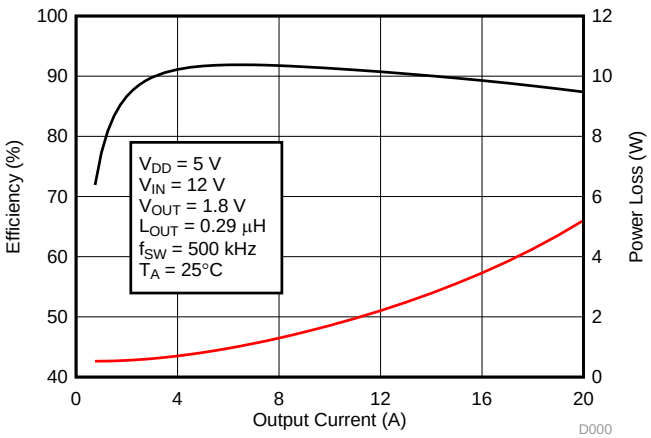
CSD97376Q4M NexFET™功率器件是经过高度优化的设计，用于高功率、高密度场合的同步降压转换器。这个产品集成了驱动器集成电路 (IC) 和 NexFET 技术来完善功率级开关功能。此驱动器 IC 具有一个内置可选二极管仿真功能，此功能可启用断续传导模式 (DCM) 运行来提升轻负载效率。此外，驱动器 IC 支持 ULQ 模式，此模式支持针对 Windows™8 的联网待机功能。借助于三态 PWM 输入，静态电流可减少至 130μA，并支持立即响应。当 SKIP# 保持在三态时，电流可减少至 8μA（恢复切换通常需要 20μs）。该组合在小型 3.5mm × 4.5mm 外形尺寸封装中实现高电流、高效率和高速开关器件。此外，PCB 封装已经过优化，可帮助减少设计时间并简化总体系统设计。

器件信息(1)

器件	数量	包装介质	封装	发货
CSD97376Q4M	2500	13 英寸卷带	3.50mm × 4.50mm SON 塑料封装	卷带封装

(1) 如需了解所有可用封装，请参阅产品说明书末尾的可订购产品附录。

典型功率级效率与功率损耗



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4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Revision A (June 2013) to Revision B **Page**

- Added description of internal connection to pin 7 in the Pin Functions table ... 3
- Added PWM line in Absolute Maximum Ratings table ... 4
- Added ESD Ratings table ... 4
- Added a NOTE to the *Application and Implementation* section ... 12
- Added *Layout* section ... 15
- 已添加 添加了*器件和文档支持* 部分 ... 17
- 已更改 将*机械数据* 部分更改成了*机械、封装和可订购信息* 部分 ... 18

Changes from Original (March 2013) to Revision A **Page**

- 更改了“特性”：从“在 15A 的电流下具有超过 90% 的系统效率”更改成了“在 15A 的电流下具有 90% 的系统效率” ... 1
- 更改了机械制图图像 ... 18
- 已添加 在机械、封装和可订购信息表中添加了尺寸行 b2 ... 18
- 更改了建议印刷电路板 (PCB) 焊盘图案图像。 ... 19
- 更改了建议模板开口图像。 ... 19

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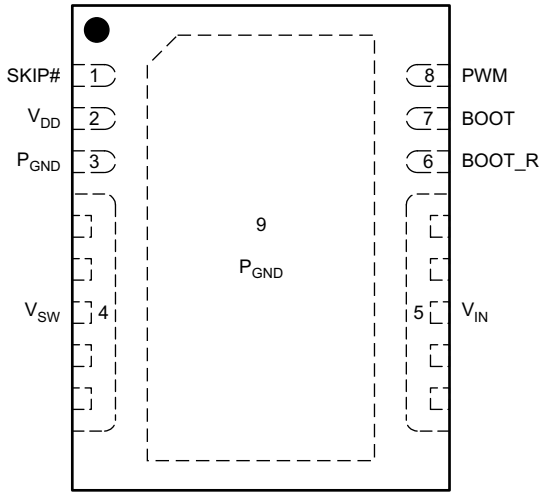
5 Pin Configuration and Functions

SON 3.5 mm × 4.5 mm
Top View



Pin Functions

PIN		DESCRIPTION
NO.	NAME	
1	SKIP#	This pin enables the diode emulation function. When this pin is held low, diode emulation mode is enabled for the sync FET. When SKIP# is high, the CSD97376Q4M operates in forced continuous conduction mode. A tri-state voltage on SKIP# puts the driver into a very low power state.
2	V_{DD}	Supply voltage to gate drivers and internal circuitry.
3	P_{GND}	Power ground. Needs to be connected to pin 9 and PCB.
4	V_{SW}	Voltage switching node. Pin connection to the output inductor.
5	V_{IN}	Input voltage pin. Connect input capacitors close to this pin.
6	BOOT_R	Bootstrap capacitor connection. Connect a minimum 0.1-µF 16-V X5R, ceramic cap from BOOT to BOOT_R pins. The bootstrap capacitor provides the charge to turn on the control FET. The bootstrap diode is integrated. BOOT_R is internally connected to V_{SW}.
7	BOOT	
8	PWM	Pulse width modulated tri-state input from external controller. Logic low sets control FET gate low and sync FET gate high. Logic high sets control FET gate high and sync FET gate low. Open or Hi-Z sets both MOSFET gates low if greater than the tri-state shutdown hold-off time (t_{3HT}).
9	P_{GND}	Power ground.

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6 Specifications

6.1 Absolute Maximum Ratings

T_A = 25°C (unless otherwise noted)(1)

		MIN	MAX	UNIT
	V_{IN} to P_{GND}	–0.3	30	V
	V_{SW} to P_{GND} , V_{IN} to V_{SW}	–0.3	30	V
	V_{SW} to P_{GND}, V_{IN} to V_{SW} (< 10 ns)	–7	33	V
	V_{DD} to P_{GND}	–0.3	6	V
	PWM, SKIP# to P_{GND}	–0.3	6	V
	BOOT to P_{GND}	–0.3	35	V
	BOOT to P_{GND} (< 10 ns)	–2	38	V
	BOOT to BOOT_R	–0.3	6	V
	BOOT to BOOT_R (duty cycle < 0.2%)		8	V
P_D	Power dissipation		8	W
T_J	Operating temperature	–40	150	°C
T_{STG}	Storage temperature	–55	150	°C

(1) Stresses above those listed in *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

T_A = 25° (unless otherwise noted)

			MIN	MAX	UNIT
V_{DD}	Gate drive voltage		4.5	5.5	V
V_{IN}	Input supply voltage			24	V
I_{OUT}	Continuous output current	V_{IN} = 12 V, V_{DD} = 5 V, V_{OUT} = 1.8 V, f_{SW} = 500 kHz, L_{OUT} = 0.29 µH(1)		20	A
I_{OUT-PK}(2)	Peak output current			45	A
f_{SW}	Switching frequency	C_{BST} = 0.1 µF (min)		2000	kHz
	On-time duty cycle			85	%
	Minimum PWM on-time		40		ns
	Operating temperature		–40	125	°C

(1) Measurement made with six 10-µF (TDK C3216X5R1C106KT or equivalent) ceramic capacitors placed across V_{IN} to P_{GND} pins.
(2) System conditions as defined in Note 1. Peak output current is applied for t_p = 10 ms, duty cycle ≤ 1%.

6.4 Thermal Information

T_A = 25°C (unless otherwise noted)

THERMAL METRIC		MIN	TYP	MAX	UNIT
$R_{\theta JC}$	Thermal resistance, junction-to-case (top of package)(1)			22.8	°C/W
$R_{\theta JB}$	Thermal resistance, junction-to-board(2)			2.5	°C/W

(1) $R_{\theta JC}$ is determined with the device mounted on a 1-in^2 (6.45-cm^2), 2-oz (0.071-mm) thick Cu pad on a 1.5-in × 1.5-in, 0.06-in (1.52-mm) thick FR4 board.
(2) $R_{\theta JB}$ value based on hottest board temperature within 1 mm of the package.

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6.5 Electrical Characteristics

T_A = 25°C, V_{DD} = POR to 5.5 V (unless otherwise noted)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
P_{LOSS}						
	Power loss(1)	V_{IN} = 12 V, V_{DD} = 5 V, V_{OUT} = 1.8 V, I_{OUT} = 12 A, f_{SW} = 500 kHz, L_{OUT} = 0.29 µH , T_J = 25°C		2.2		W
	Power loss(2)	V_{IN} = 19 V, V_{DD} = 5 V, V_{OUT} = 1.8 V, I_{OUT} = 12 A, f_{SW} = 500 kHz, L_{OUT} = 0.29 µH , T_J = 25°C		2.4		W
	Power loss(2)	V_{IN} = 19 V, V_{DD} = 5 V, V_{OUT} = 1.8 V, I_{OUT} = 12 A, f_{SW} = 500 kHz, L_{OUT} = 0.29 µH , T_J = 125°C		3		W
V_{IN}						
I_Q	V_{IN} quiescent current	PWM = floating, V_{DD} = 5 V, V_{IN} = 24 V			1	µA
V_{DD}						
I_{DD}	Standby supply current	PWM = float, SKIP# = V_{DD} or 0 V		130		µA
		SKIP# = float		8		
I_{DD}	Operating supply current	PWM = 50% duty cycle, f_{SW} = 500 kHz		5.3		mA
POWER-ON RESET AND UNDERVOLTAGE LOCKOUT						
V_{DD} rising	Power-on reset				4.15	V
V_{DD} falling	UVLO		3.7			V
	Hysteresis			0.2		mV
PWM AND SKIP# I/O SPECIFICATIONS						
R_I	Input impedance	Pullup to V_{DD}		1700		kΩ
		Pulldown (to GND)		800		
V_{IH}	Logic level high		2.65			V
V_{IL}	Logic level low				0.6	V
V_{IH}	Hysteresis			0.2		V
V_{TS}	Tri-state voltage		1.3		2	V
$t_{THOLD(off1)}$	Tri-state activation time (falling) PWM			60		ns
$t_{THOLD(off2)}$	Tri-state activation time (rising) PWM			60		ns
t_{TSKF}	Tri-state activation time (falling) SKIP#			1		µs
t_{TSKR}	Tri-state activation time (rising) SKIP#			1		µs
$t_{3RD(PWM)}$(2)	Tri-state exit time PWM				100	ns
$t_{3RD(SKIP\#)}$(2)	Tri-state exit time SKIP#				50	µs
BOOTSTRAP SWITCH						
V_{FBST}	Forward voltage	I_F = 10 mA		120	240	mV
I_{RLEAK}(2)	Reverse leakage	V_{BST} – V_{DD} = 25 V			2	µA

(1) Measurement made with six 10 µF (TDK C3216X5R1C106KT or equivalent) ceramic capacitors placed across V_{IN} to P_{GND} pins.
(2) Specified by design.

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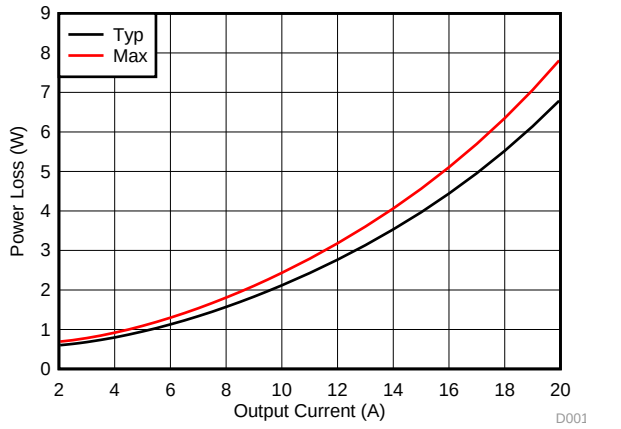
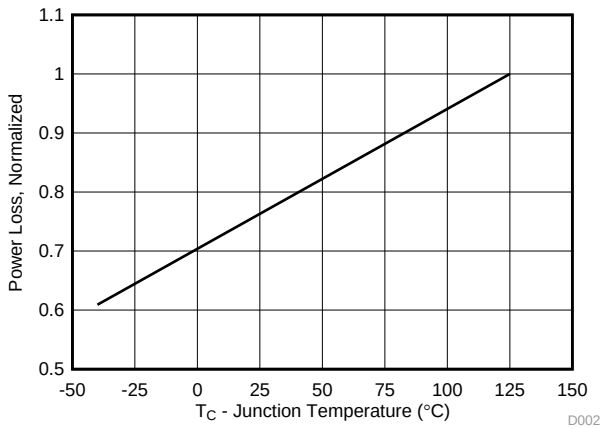
6.6 Typical Characteristics

T_J = 125°C, unless stated otherwise.



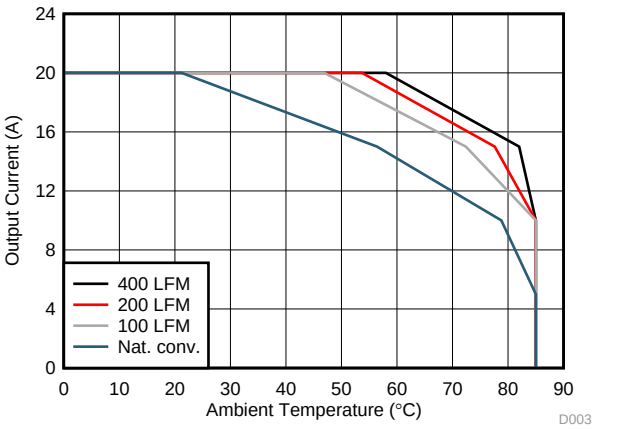
V_{IN} = 12 V V_{DD} = 5 V V_{OUT} = 1.8 V
f_{SW} = 500 kHz L_{OUT} = 0.29 µH

Figure 1. Power Loss vs Output Current



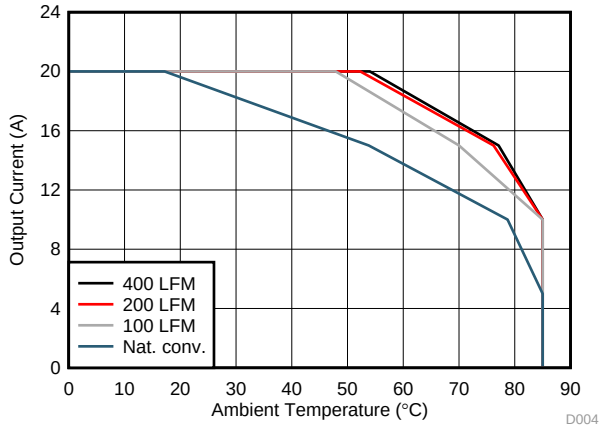
V_{IN} = 12 V V_{DD} = 5 V V_{OUT} = 1.8 V
f_{SW} = 500 kHz L_{OUT} = 0.29 µH

Figure 2. Power Loss vs Temperature



V_{IN} = 12 V V_{DD} = 5 V V_{OUT} = 1.8 V
f_{SW} = 500 kHz L_{OUT} = 0.29 µH

Figure 3. Safe Operating Area – PCB Horizontal Mount (1)



V_{IN} = 12 V V_{DD} = 5 V V_{OUT} = 1.8 V
f_{SW} = 500 kHz L_{OUT} = 0.29 µH

Figure 4. Safe Operating Area – PCB Vertical Mount (1)

(1) The Typical CSD97376Q4M system characteristic curves are based on measurements made on a PCB design with dimensions of 4 in (W) x 3.5 in (L) x 0.062 in (T) and 6 copper layers of 1-oz copper thickness. See the *Application and Implementation* section for detailed explanation.

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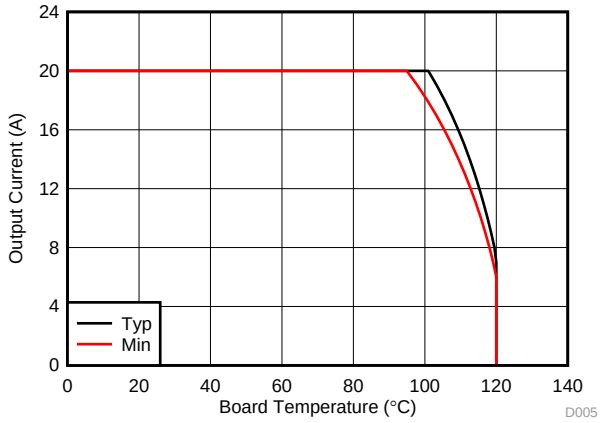
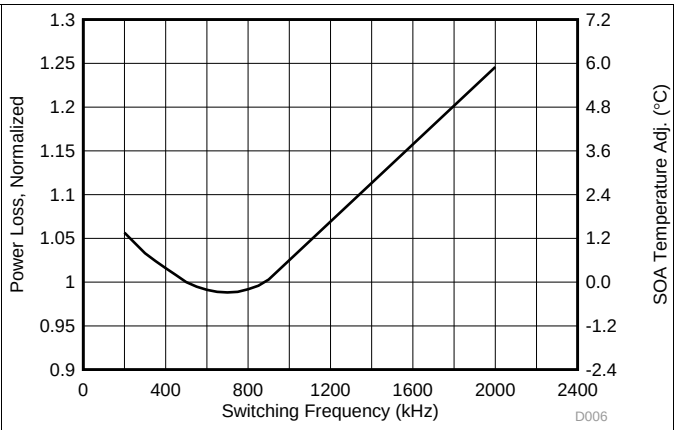
Typical Characteristics (continued)

T_J = 125°C, unless stated otherwise.



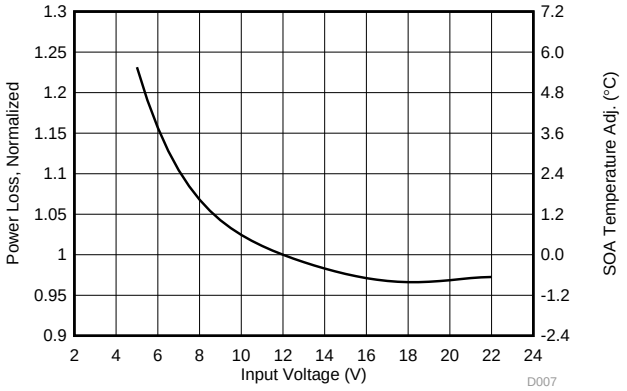
V_{IN} = 12 V V_{DD} = 5 V V_{OUT} = 1.8 V
f_{SW} = 500 kHz L_{OUT} = 0.29 µH

Figure 5. Typical Safe Operating Area (1)



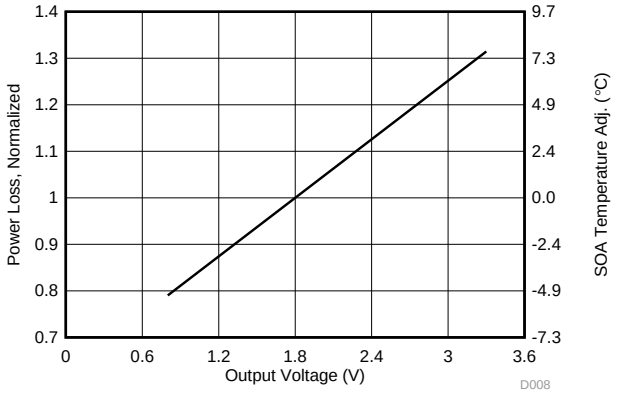
V_{IN} = 12 V V_{DD} = 5 V V_{OUT} = 1.8 V
I_{OUT} = 20 A L_{OUT} = 0.29 µH

Figure 6. Normalized Power Loss vs Frequency



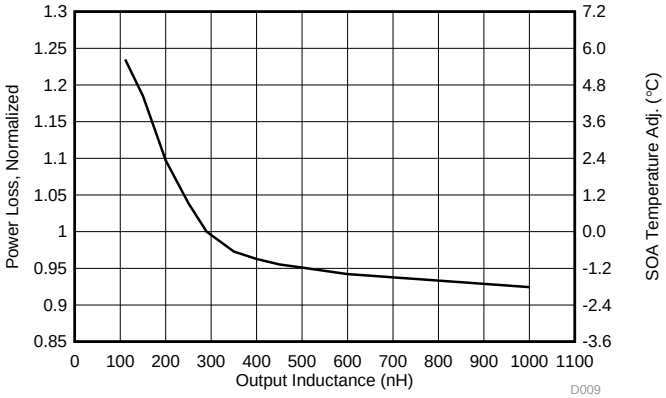
f_{SW} = 500 kHz V_{DD} = 5 V V_{OUT} = 1.8 V
I_{OUT} = 20 A L_{OUT} = 0.29 µH

Figure 7. Normalized Power Loss vs Input Voltage



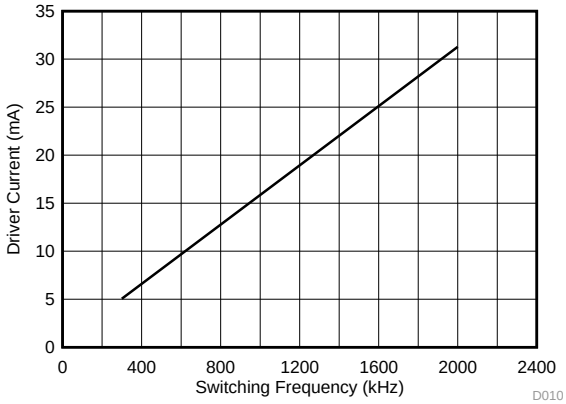
V_{IN} = 12 V V_{DD} = 5 V f_{SW} = 500 kHz
I_{OUT} = 20 A L_{OUT} = 0.29 µH

Figure 8. Normalized Power Loss vs Output Voltage



V_{IN} = 12 V V_{DD} = 5 V V_{OUT} = 1.8 V
f_{SW} = 500 kHz I_{OUT} = 20 A

Figure 9. Normalized Power Loss vs Output Inductance



V_{IN} = 12 V V_{DD} = 5 V V_{OUT} = 1.8 V
I_{OUT} = 20 A L_{OUT} = 0.29 µH

Figure 10. Driver Current vs Frequency

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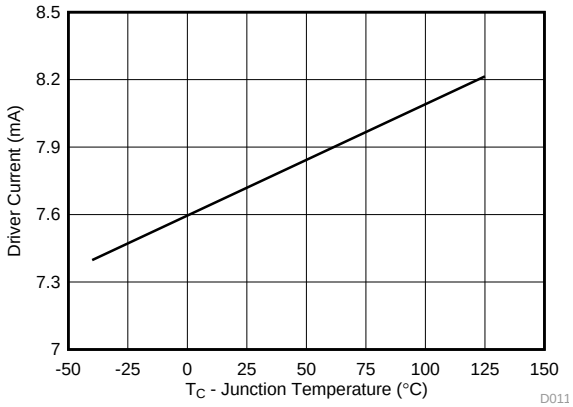
Typical Characteristics (continued)

T_J = 125°C, unless stated otherwise.



V_{IN} = 12 V
I_{OUT} = 20 A
V_{DD} = 5 V
L_{OUT} = 0.29 µH
V_{OUT} = 1.8 V

Figure 11. Driver Current vs Temperature

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7 Detailed Description

7.1 Functional Block Diagram

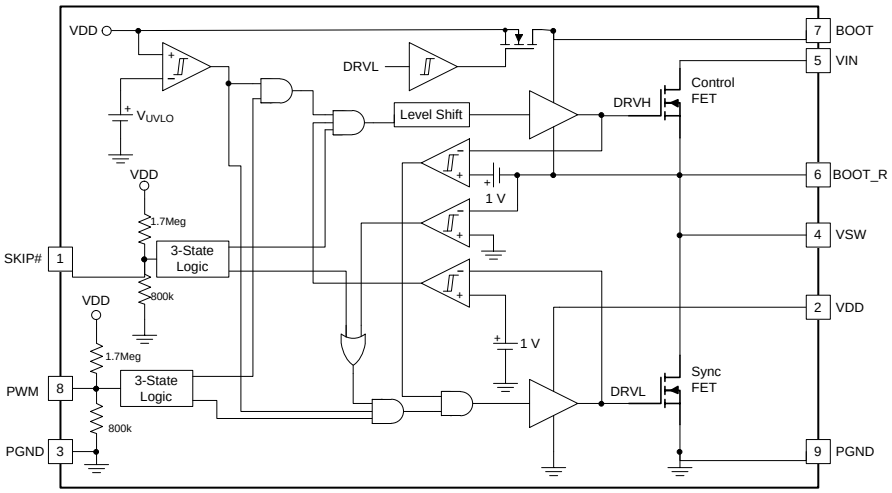

Figure 12. Functional Block Diagram

7.2 Powering CSD97376Q4M and Gate Drivers

An external V_{DD} voltage is required to supply the integrated gate driver IC and provide the necessary gate drive power for the MOSFETS. A 1-µF 10-V X5R or higher ceramic capacitor is recommended to bypass V_{DD} pin to P_{GND}. A bootstrap circuit to provide gate drive power for the control FET is also included. The bootstrap supply to drive the control FET is generated by connecting a 100-nF 16-V X5R ceramic capacitor between BOOT and BOOT_R pins. An optional R_{BOOT} resistor can be used to slow down the turnon speed of the control FET and reduce voltage spikes on the V_{SW} node. A typical 1-Ω to 4.7-Ω value is a compromise between switching loss and V_{SW} spike amplitude.

7.3 Undervoltage Lockout Protection (UVLO)

The undervoltage lockout (UVLO) comparator evaluates the VDD voltage level. As V_{VDD} rises, both the control FET and sync FET gates hold actively low at all times until V_{VDD} reaches the higher UVLO threshold (V_{UVLO_H}). Then the driver becomes operational and responds to PWM and SKIP# commands. If VDD falls below the lower UVLO threshold (V_{UVLO_L} = V_{UVLO_H} – hysteresis), the device disables the driver and drives the outputs of the control FET and sync FET gates actively low. Figure 13 shows this function.

CAUTION

Do not start the driver in the very low power mode (SKIP# = tri-state).

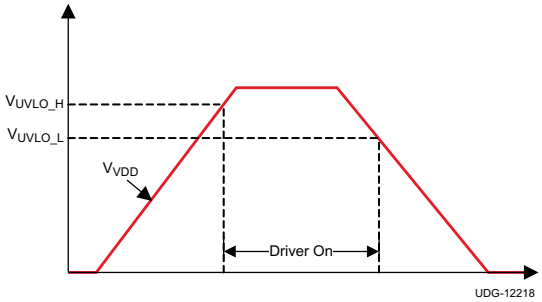

Figure 13. UVLO Operation

7.4 PWM Pin

The PWM pin incorporates an input tri-state function. The device forces the gate driver outputs to low when PWM is driven into the tri-state window and the driver enters a low-power state with zero exit latency. The pin incorporates a weak pullup to maintain the voltage within the tri-state window during low-power modes. Operation into and out of tri-state mode follows the timing diagram outlined in Figure 14.

When VDD reaches the UVLO_H level, a tri-state voltage range (window) is set for the PWM input voltage. The window is defined the PWM voltage range between PWM logic high (V_{IH}) and logic low (V_{IL}) thresholds. The device sets high-level input voltage and low-level input voltage threshold levels to accommodate both 3.3-V (typical) and 5-V (typical) PWM drive signals.

When the PWM exits tri-state, the driver enters CCM for a period of 4 µs, regardless of the state of the SKIP# pin. Normal operation requires this time period in order for the auto-zero comparator to resume.

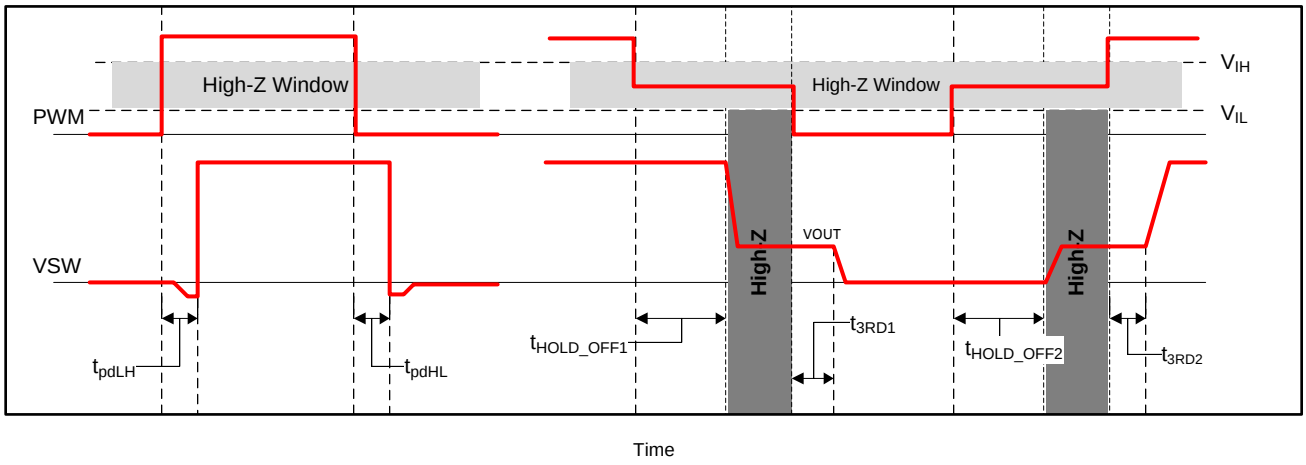

Figure 14. PWM Tri-State Timing Diagram

7.5 SKIP# Pin

The SKIP# pin incorporates the input tri-state buffer as PWM. The function is somewhat different. When SKIP# is low, the zero crossing (ZX) detection comparator is enabled, and DCM mode operation occurs if the load current is less than the critical current. When SKIP# is high, the ZX comparator disables, and the converter enters FCCM mode. When both SKIP# and PWM are tri-stated, normal operation forces the gate driver outputs low and the driver enters a low-power state. In the low-power state, the UVLO comparator remains off to reduce quiescent current. When SKIP# is pulled low, the driver wakes up and is able to accept PWM pulses in less than 50 µs.

Table 1 shows the logic functions of UVLO, PWM, SKIP#, the control FET gate and the sync FET gate.

Table 1. Logic Functions of the Driver IC

UVLO	PWM	SKIP#	SYNC FET GATE	CONTROL FET GATE	MODE
Active	—	—	Low	Low	Disabled
Inactive	Low	Low	High(1)	Low	DCM(1)
Inactive	Low	High	High	Low	FCCM
Inactive	High	H or L	Low	High	
Inactive	Tri-state	H or L	Low	Low	LQ
Inactive	—	Tri-state	Low	Low	ULQ

(1) Until zero crossing protection occurs.

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7.5.1 Zero Crossing (ZX) Operation

The zero crossing comparator is adaptive for improved accuracy. As the output current decreases from a heavy load condition, the inductor current also reduces and eventually arrives at a *valley*, where it touches zero current, which is the boundary between continuous conduction and discontinuous conduction modes. The SW pin detects the zero-current condition. When this zero inductor current condition occurs, the ZX comparator turns off the rectifying MOSFET.

7.6 Integrated Boost-Switch

To maintain a BST-SW voltage close to VDD (to get lower conduction losses on the high-side FET), the conventional diode between the VDD pin and the BST pin is replaced by a FET which is gated by the DRVL signal.

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8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The power stage CSD97376Q4M is a highly optimized design for synchronous buck applications using NexFET devices with a 5-V gate drive. The control FET and sync FET silicon are parametrically tuned to yield the lowest power loss and highest system efficiency. As a result, a rating method is used that is tailored towards a more systems-centric environment. The high-performance gate driver IC integrated in the package helps minimize the parasitics and results in extremely fast switching of the power MOSFETs. System-level performance curves such as power loss, safe operating area and normalized graphs allow engineers to predict the product performance in the actual application.

8.2 Power Loss Curves

MOSFET centric parameters such as $R_{DS(ON)}$ and Q_{gd} are primarily needed by engineers to estimate the loss generated by the devices. In an effort to simplify the design process for engineers, Texas Instruments has provided measured power loss performance curves. Figure 1 plots the power loss of the CSD97376Q4M as a function of load current. This curve is measured by configuring and running the CSD97376Q4M as it would be in the final application (see Figure 15). The measured power loss is the CSD97376Q4M device power loss which consists of both input conversion loss and gate drive loss. Equation 1 is used to generate the power loss curve.

$$\text{Power loss} = (V_{IN} \times I_{IN}) + (V_{DD} \times I_{DD}) - (V_{SW_AVG} \times I_{OUT}) \quad (1)$$

The power loss curve in Figure 1 is measured at the maximum recommended junction temperature of T_J = 125°C under isothermal test conditions.

8.3 Safe Operating Curves (SOA)

The SOA curves in the CSD97376Q4M data sheet give engineers guidance on the temperature boundaries within an operating system by incorporating the thermal resistance and system power loss. Figure 3 and Figure 5 outline the temperature and airflow conditions required for a given load current. The area under the curve dictates the safe operating area. All the curves are based on measurements made on a PCB design with dimensions of 4 in (W) × 3.5 in (L) × 0.062 in (T) and 6 copper layers of 1-oz copper thickness.

8.4 Normalized Curves

The normalized curves in the CSD97376Q4M data sheet give engineers guidance on the power loss and SOA adjustments based on their application specific needs. These curves show how the power loss and SOA boundaries will adjust for a given set of systems conditions. The primary Y-axis is the normalized change in power loss and the secondary Y-axis is the change is system temperature required in order to comply with the SOA curve. The change in power loss is a multiplier for the power loss curve and the change in temperature is subtracted from the SOA curve.

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Normalized Curves (continued)

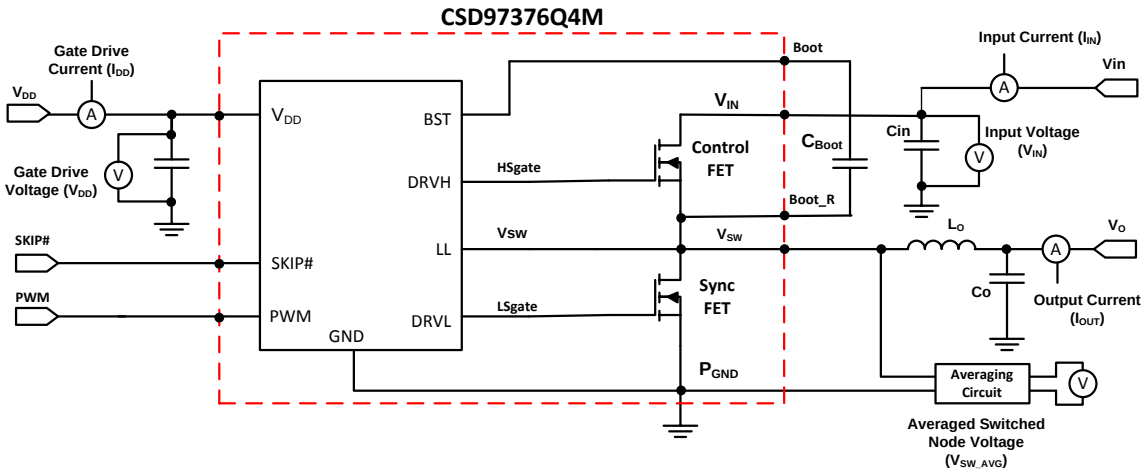

Figure 15. Power Loss Test Circuit

8.5 Calculating Power Loss and SOA

The user can estimate product loss and SOA boundaries by arithmetic means (see *Design Example*). Though the power loss and SOA curves in this data sheet are taken for a specific set of test conditions, the following procedure will outline the steps engineers should take to predict product performance for any set of system conditions.

8.5.1 Design Example

Operating conditions: output current (I_{OUT}) = 10 A, input voltage (V_{IN}) = 7 V, output voltage (V_{OUT}) = 1.5 V, switching frequency (f_{SW}) = 800 kHz, output inductor (L_{OUT}) = 0.2 µH

8.5.2 Calculating Power Loss

- Typical power loss at 10 A = 2.1 W (Figure 1)
- Normalized power loss for switching frequency ≈ 0.99 (Figure 6)
- Normalized power loss for input voltage ≈ 1.1 (Figure 7)
- Normalized power loss for output voltage ≈ 0.93 (Figure 8)
- Normalized power loss for output inductor ≈ 1.1 (Figure 9)
- **Final calculated power loss = 2.1 W × 0.99 × 1.1 × 0.93 × 1.1 ≈ 2.3 W**

8.5.3 Calculating SOA Adjustments

- SOA adjustment for switching frequency ≈ -0.2°C (Figure 6)
- SOA adjustment for input voltage ≈ 2.5°C (Figure 7)
- SOA adjustment for output voltage ≈ 1°C (Figure 8)
- SOA adjustment for output inductor ≈ 2.3°C (Figure 9)
- **Final calculated SOA adjustment = -0.2 + 2.5 + (-1.5) + 2.3 ≈ 3.1°C**

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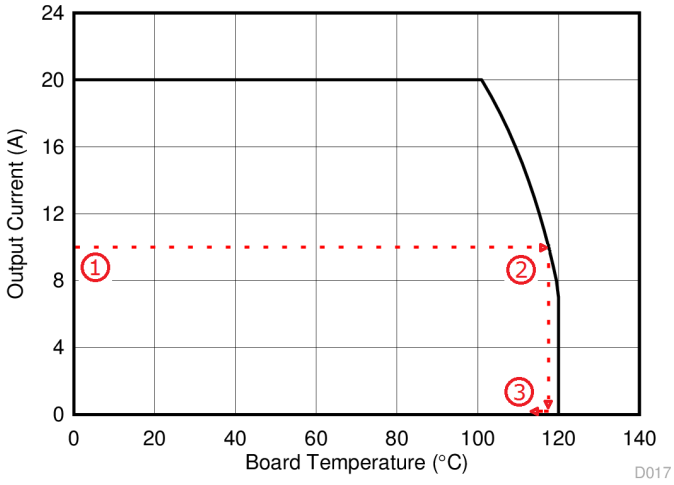
Calculating Power Loss and SOA (continued)



V_{IN} = 12 V V_{DD} = 5 V V_{OUT} = 1.8 V f_{SW} = 500 kHz L_{OUT} = 0.29 µH

Figure 16. Power Stage CSD97376Q4M SOA

In the design example above, the estimated power loss of the CSD97376Q4M would increase to 2.3 W. In addition, the maximum allowable board and/or ambient temperature would have to decrease by 3.1°C. Figure 16 graphically shows how the SOA curve would be adjusted accordingly.

1. Start by drawing a horizontal line from the application current to the SOA curve.
2. Draw a vertical line from the SOA curve intercept down to the board/ambient temperature.
3. Adjust the SOA board/ambient temperature by subtracting the temperature adjustment value.

In the design example, the SOA temperature adjustment yields a reduction in allowable board/ambient temperature of 3.1°C. In the event the adjustment value is a negative number, subtracting the negative number would yield an increase in allowable board/ambient temperature.

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9 Layout

9.1 Layout Guidelines

9.1.1 Recommended PCB Design Overview

There are two key system-level parameters that can be addressed with a proper PCB design: electrical and thermal performance. Properly optimizing the PCB layout will yield maximum performance in both areas. Below is a brief description on how to address each parameter.

9.1.2 Electrical Performance

The CSD97376Q4M has the ability to switch at voltage rates greater than 10 kV/µs. Special care must be then taken with the PCB layout design and placement of the input capacitors, inductor and output capacitors.

- The placement of the input capacitors relative to V_{IN} and P_{GND} pins of CSD97376Q4M device should have the highest priority during the component placement routine. It is critical to minimize these node lengths. As such, ceramic input capacitors need to be placed as close as possible to the V_{IN} and P_{GND} pins (see Figure 17). The example in Figure 17 uses 1 × 1-nF 0402 25-V and 3 × 10-µF 1206 25-V ceramic capacitors (TDK Part # C3216X5R1C106KT or equivalent). Notice there are ceramic capacitors on both sides of the board with an appropriate amount of vias interconnecting both layers. In terms of priority of placement next to the power stage C5, C8 and C6, C19 should follow in order.
- The bootstrap cap C_{BOOT} 0.1-µF 0603 16-V ceramic capacitor should be closely connected between BOOT and BOOT_R pins.
- The switching node of the output inductor should be placed relatively close to the power stage CSD97376Q4M V_{SW} pins. Minimizing the V_{SW} node length between these two components will reduce the PCB conduction losses and actually reduce the switching noise level. (1)

9.1.3 Thermal Performance

The CSD97376Q4M has the ability to use the GND planes as the primary thermal path. As such, the use of thermal vias is an effective way to pull away heat from the device and into the system board. Concerns of solder voids and manufacturability problems can be addressed by the use of three basic tactics to minimize the amount of solder attach that will wick down the via barrel:

- Intentionally space out the vias from each other to avoid a cluster of holes in a given area.
- Use the smallest drill size allowed in your design. The example in Figure 17 uses vias with a 10-mil drill hole and a 16-mil capture pad.
- Tent the opposite side of the via with solder-mask.

In the end, the number and drill size of the thermal vias should align with the end user's PCB design rules and manufacturing capabilities.

(1) Keong W. Kam, David Pommerenke, "EMI Analysis Methods for Synchronous Buck Converter EMI Root Cause Analysis", University of Missouri – Rolla

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9.2 Layout Example

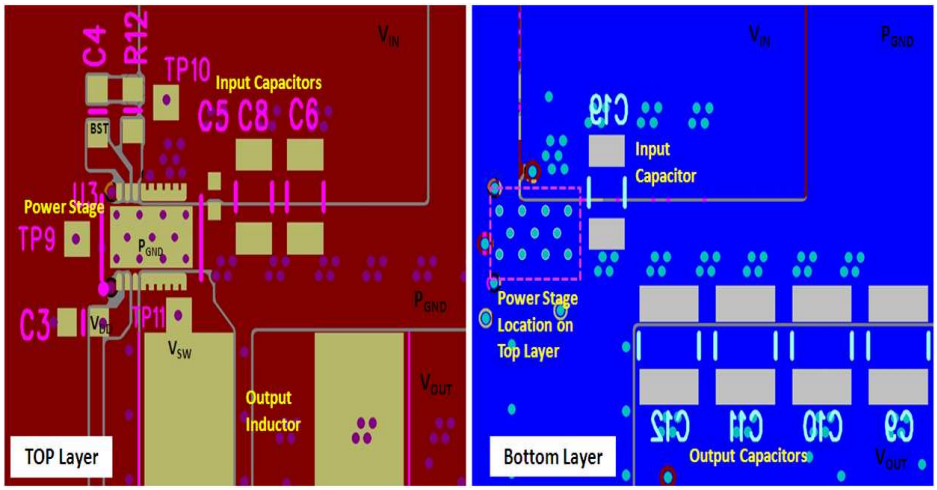

Figure 17. Recommended PCB Layout (Top Down View)

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10 器件和文档支持

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10.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

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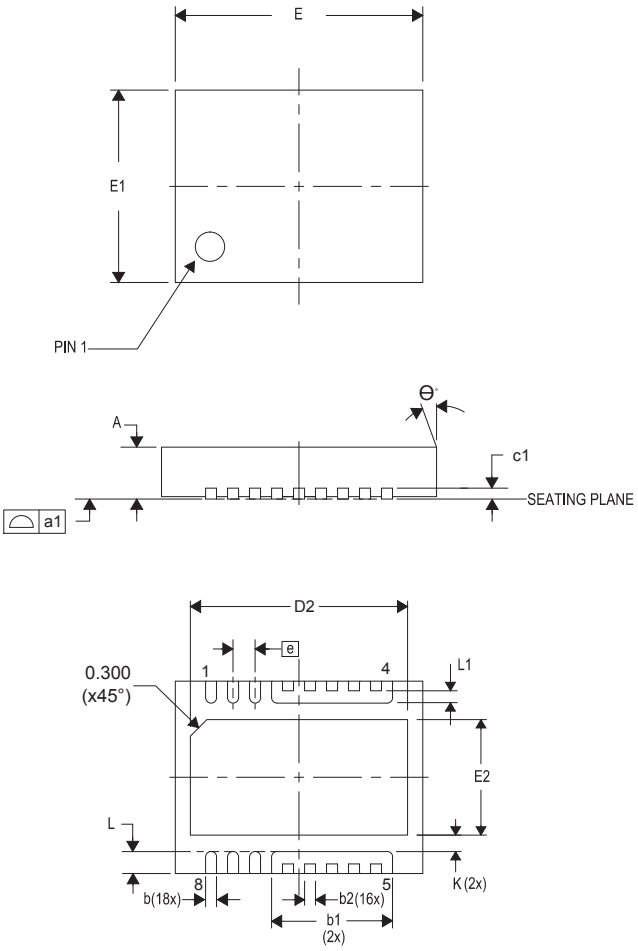
11 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知和修订此文档。如欲获取此产品说明书的浏览器版本，请参阅左侧的导航。

11.1 封装尺寸



DIM	毫米			英寸		
	最小值	标称值	最大值	最小值	标称值	最大值
A	0.800	0.900	1.000	0.031	0.035	0.039
a1	0.000	0.000	0.080	0.000	0.000	0.003
b	0.150	0.200	0.250	0.006	0.008	0.010
b1	2.000	2.200	2.400	0.079	0.087	0.095
b2	0.150	0.200	0.250	0.006	0.008	0.010
c1	0.150	0.200	0.250	0.006	0.008	0.010
D2	3.850	3.950	4.050	0.152	0.156	0.160
E	4.400	4.500	4.600	0.173	0.177	0.181
E1	3.400	3.500	3.600	0.134	0.138	0.142
E2	2.000	2.100	2.200	0.079	0.083	0.087
e		0.400 典型值			0.016 典型值	
K		0.300 典型值			0.012 典型值	
L	0.300	0.400	0.500	0.012	0.016	0.020

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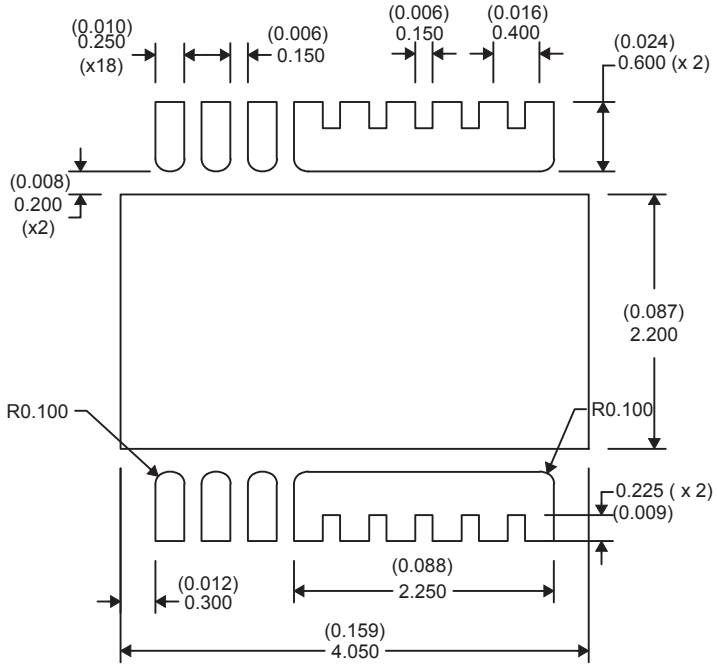
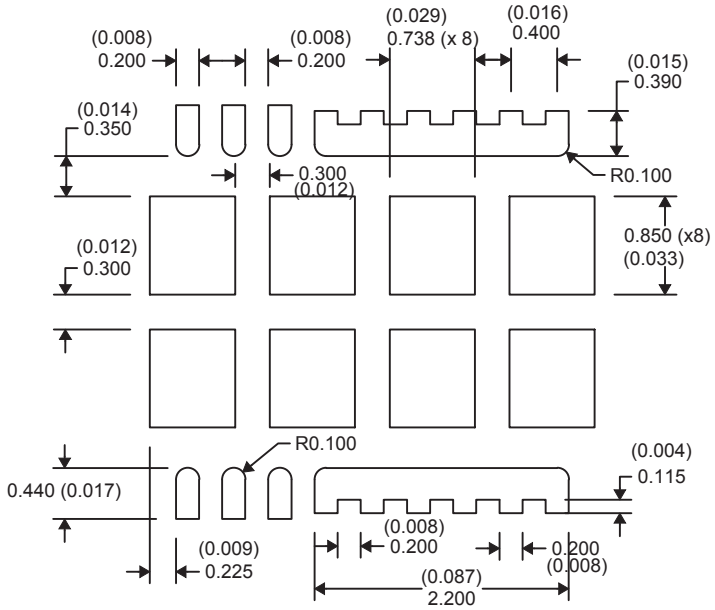
DIM	毫米			英寸		
	最小值	标称值	最大值	最小值	标称值	最大值
L1	0.180	0.230	0.280	0.007	0.009	0.011
θ	0.00	—	—	0.00	—	—

11.2 建议印刷电路板 (PCB) 焊盘图案



11.3 建议模板开口



NOTE: 尺寸单位为 mm（英寸）。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CSD97376Q4M	ACTIVE	VSON-CLIP	DPC	8	2500	RoHS-Exempt & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 150	97376M	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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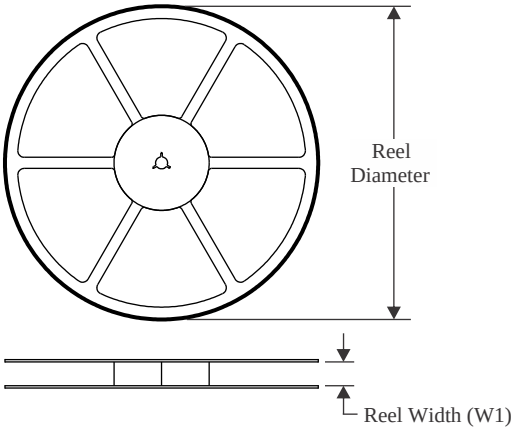
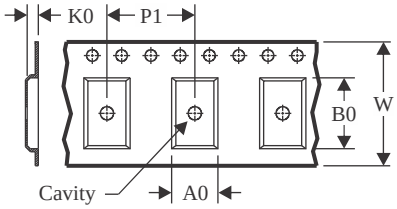
TAPE AND REEL INFORMATION

REEL DIMENSIONS

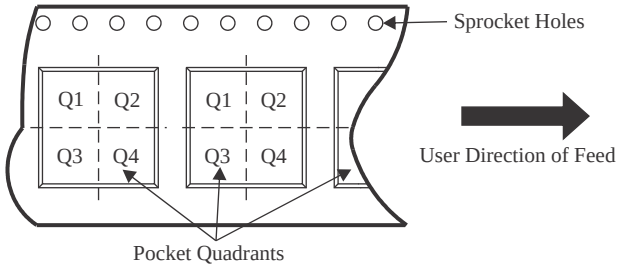


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

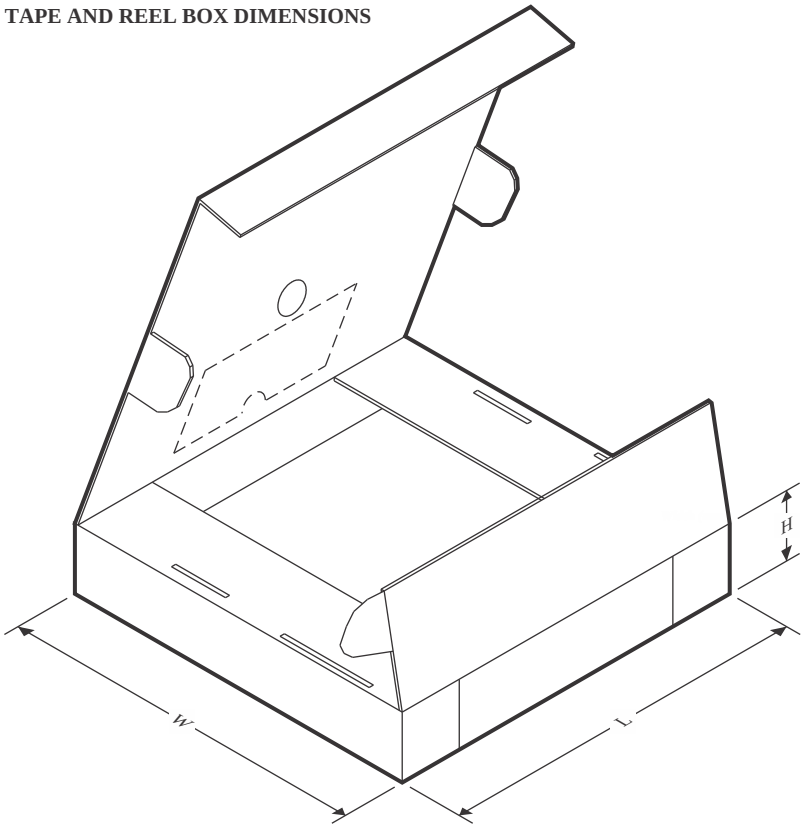
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CSD97376Q4M	VSON-CLIP	DPC	8	2500	330.0	12.4	3.71	4.71	1.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CSD97376Q4M	VSON-CLIP	DPC	8	2500	346.0	346.0	33.0

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